University / Academy: Arab Academy for Science and Technology & Maritime Transport
Faculty / Institute: College of Computing and Information Technology
Program: Computer Science / Information Systems / Software Engineering

Form No. (12)
Course Specification

1- Course Data

Course Code: CE216	Course Title: **Digital Logic Design**	Academic Year / Level: Year 2 / Semester 3
Specialization: Computer Science	No. of Instructional Units: 2 hrs lecture 2 hrs lab 2 hrs section	Lecture:

2- Course Aim	This course aims to develop engineering skills in the design and analysis of digital logic circuits with applications to digital computer. It covers: Number systems, binary arithmetic and codes, logic gates, Boolean algebra and logic simplifications, Design and realization of combinational circuits, Functions of combinational circuits logic: Flip-Flops, analysis design and realization of counters, analysis and realization of shift registers, Computer – aided engineering
3- Intended Learning Outcome:	
a- Knowledge and Understanding	**Students will be able to demonstrate knowledge of:** K1. Essential facts, concepts, principles and theories relating to computing and information and computer applications as appropriate to the program of study. K4. Criteria and specifications appropriate to specific problems, and plan strategies for their solution. K6. The current and underlying technologies that support computer processing and inter-computer communication. • Define digital and analog concepts.(K1) • Describe Logic levels and digital waveforms. .(K1) • Describe various parameters of a pulse waveform and explain the basic logic operation. .(K1) • List different number systems (Decimal, Binary, Octal and Hexadecimal). .(K1) • Explain the conversion process between number systems. .(K1) • Explain the binary arithmetic (addition, subtraction, multiplication and division) for signed and unsigned binary numbers. .(K1) • List different codes (Gray code, Excess-3 code, Binary Coded Decimal). .(K1) • Define the logic gate concept. (K4,K6) • Describe different types of logic gates (AND, OR, NOT, NAND, Negative

	OR, NOR, Negative AND, Exclusive OR and Exclusive NOR). (K4,K6) • Describe laws and rules of Boolean algebra. (K4,K6) • Explain how to simplify the Boolean expression using Boolean algebra technique. (K4,K6) • Show the standard forms of Boolean expressions (Sum of Products form and Product of Sums form). (K4,K6) • Explain how to simplify the Boolean expression using KARNAUGH map. (K4,K6) • Describe the Universal Gates (NAND, NOR). (K4,K6) • Describe the basic Adders (Half Adder and Full Adder) (K4,K6) • Explain Binary Parallel Adder. (K4,K6) • Describe Carry Look Ahead Adder. (K4,K6) • Describe the comparator circuit. (K4,K6) • Explain different types of Decoders and show their applications. (K4,K6) • Explain different types of Encoders and show their applications. (K4,K6) • Explain different types of Multiplexers and show their applications. (K4,K6) • Explain different types of De-multiplexers and show their applications. (K4,K6) • Explain different types of Latches (S-R Latch, Gated S-R Latch and Gated D-Latch) and show their applications. (K4,K6) • Explain different types of Edge Triggered Flip-Flops (S-R Flip-Flop) and show their applications. (K4,K6) • Explain different types of Edge Triggered Flip-Flops (D Flip-Flop and J-K Flip-Flop) and show their applications. (K4,K6) • Describe the asynchronous and synchronous binary counters. (K4,K6) • Explain the synchronous counter design. (K4,K6) • Explain the up/down counters. (K4,K6) • Describe the shift register basics. (K4,K6) • List the types of shift register (serial in/ serial out, serial in/ parallel out, parallel in/ serial out and parallel in / parallel out). (K4,K6)
b- Intellectual Skills	**By the end of the course, the student acquires high skills and an ability to understand:** I2. Realize the concepts, principles, theories and practices behind computing and information as an academic discipline. I11. Perform comparisons between (algorithms, methods, techniques...etc). I13. Identify attributes, components, relationships, patterns, main ideas, and errors. (Equivalent to I12 in the IS and SE departments) Assess the period, frequency, Pulse Width and duty cycle for different waveforms. (I2) • Apply the conversions of numbers from one number system to another one. (I2) • Perform the binary arithmetic operations on the signed and unsigned binary numbers. (I2) • Apply the code conversions from any certain code to another. (I2) • Determine the truth table for each logic gate.(I2,I11,I13) • Demonstrate the output waveforms for different logic gates. .(I2,I11,I13) • Simplify Boolean expressions using Boolean algebra techniques.(I2) • Apply DEMORGAN'S Theorems for Boolean expressions. .(I2) • Construct the truth table for sum of products and product of sums. .(I2) • Simplify Boolean expressions using KARNAUGH map. .(I2) • Implement Boolean expressions using universal gates. .(I2) • Construct the truth table for the Half and Full Adder. .(I2) • Design Full Adder using Half Adder. (I2,I13) • Design parallel adder. (I2,I13) • Demonstrate the output waveforms for parallel adder. (I2,I13) • Demonstrate the internal architecture of the decoder. (I2,I13) • Show how to expand the 3-8 Decoder to obtain the 4-16 Decoder. (I2,I13) • Demonstrate the internal architecture of the Encoder. (I2,I13)

	• Show how to expand the 8-3 Encoder to obtain the 16-4 Encoder. (I2,I13) • Demonstrate the internal architecture of the Multiplexer. (I2,I13) • Show how to expand the 8-1 Multiplexer to obtain the 16-1 Multiplexer. (I2,I13) • Demonstrate the internal architecture of the DEMULTIPLXER. (I2,I13) • Demonstrate the internal architecture of the S-R Latch. (I11,I13) • Determine the output waveform for S-R latch. (I11,I13) • Demonstrate the internal architecture of the Gated S-R Latch. (I11,I13) • Determine the output waveform for Gated S-R latch. (I11,I13) • Demonstrate the internal architecture of the Gated D Latch. (I11,I13) • Determine the output waveform for Gated D latch. (I11,I13) • Demonstrate the internal architecture of the S-R flip-flop. (I11,I13) • Determine the output waveform for S-R flip-flop. (I11,I13) • Demonstrate the internal architecture of the D flip-flop. (I11,I13) • Determine the output waveform for D flip-flop. (I11,I13) • Demonstrate the internal architecture of the J-K flip-flop. (I11,I13) • Determine the output waveform for J-K flip-flop. (I11,I13) • Demonstrate the internal architecture of the asynchronous and synchronous counters. (I11,I13) • Demonstrate the internal architecture of different types of shift registers. (I11,I13)
c- Professional Skills	**By the end of the course the student will have the ability to:** P1. Operate computing equipment, recognizing its logical and physical properties, capabilities and limitations. P7. Assess the implications, risks or safety aspects involved in the operation of computing equipment within a specific context. • Design 4X1 Multiplexer and 1X4 DEMULTIPLEXER. • Design a DECADE counter. • Design an irregular counter. • Design the up/down counter. • Connect a switch to a L.E.D on the breadboard to examine the effect of Binary 1 and Binary 0 on the L.E.D. • Connect ICs that contain several Logic Gates and examine the output on the L.E.D. • Connect the Half Adder and the Full Adder Circuits. • Connect a 2-Bit Adder. • Connect 1-Bit and 2-Bit Comparators. • Connect BCD to 7-Segment Decoder/Driver (0 to 9) and examine the output on the 7-segment display. • Connect BCD to 7-Segment Decoder/Driver (A to F) and examine the output on the 7-segment display. • Connect BCD To 7-Segment Decoder/Driver (0 to F) and examine the output on the 7-segment display. • Connect the of 555 Timer Acts as Oscillator (ASTABLE State). • Connect a 2-Bit Asynchronous Counter and examine the output on the 7-segment display.
d- General Skills	**Students will be able to:** G1. Demonstrate the ability to make use of a range of learning resources and to manage one's own learning. G2. Show the use of information-retrieval. G3. Demonstrate skills in group working, team management, time

	management and organizational skills. • Verify theory with practice. • Apply skills learned to undertake small-scale practical projects
4- Course Content	<table><tr><th>#</th><th>CLO</th></tr><tr><td>1</td><td>1. Know the basic differences between analog and digital systems</td></tr><tr><td>2</td><td>2. Use binary numbers and codes</td></tr><tr><td>3</td><td>Describe the operation of logic gates</td></tr><tr><td>4</td><td>Apply Boolean Algebra on K-map</td></tr><tr><td>5</td><td>Describing circuit operations using state diagrams</td></tr><tr><td>6</td><td>Design a combinational and sequential logic circuits to simplify function</td></tr></table>
5- Teaching and Learning Methods	Lectures, Labs, Projects, Individual study & self-learning.
6- Teaching and Learning Methods for Students with Special Needs	• Students with special needs are requested to contact the college representative for special needs (currently Dr Hoda Mamdouh in room C504) • Consulting with lecturer during office hours. • Consulting with teaching assistant during office hours. • Private Sessions for redelivering the lecture contents. • For handicapped accessibility, please refer to program specification..
7- Student Assessment:	
a- Procedures used:	Exams and Individual Projects
b- Schedule:	Week 7 exam Projects through the semester Week 16Final exam
c- Weighing of Assessment:	7^{th} week exam 30% 12^{th} Week exam 20% Lab work 10% Final exam 40%
8- List of References:	
a- Course Notes	From the Moodle on www.aast.edu
b- Required Books (Textbooks)	Thomas L. Floyd, *Digital Fundamentals* (9th Edition), Prentice Hall
c- Recommended Books	• M. Mano, Digital Design, 3rd Edition, Prentice Hall, 2002. • J. P. Hayes, Introduction to Digital Logic Design, Addison Wesley, 1993. • John F. Wakerly, Digital Design Principles and Practices, 4th

	Edition, Prentice Hall, 2005.
d- Periodicals, Web Sites, ..., etc.	

Course Instructor: Dr Waleed Fakhr Head of Department: Dr Samah Senbel

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