CC 523 – Computer Design and Performance Evaluation

COURSE INFORMATION

Course Title: Computer Design and Performance Evaluation

Code: CC 523

Hours: Lecture – 2 Hrs. Tutorial / lab – 2 / 2 Hrs. Credit – 3.

Prerequisite: CC 311.

GRADING

Class Performance/Attendance:	10%
Midterm # 1/Assignments – (7th Week):	30%
Midterm # 2/Assignments – (12th Week):	20%
Final Exam:	40%

COURSE DESCRIPTION

Comparison between the two major design methodologies based on ISA (Instruction Set Architecture) and ASA (Application Specific Architecture). The course covers the topics of queuing theory and Markov processes as a tool for computer system performance evaluation. Moreover, the students are introduced to operational analysis techniques regarding performance of computer systems.

TEXT BOOK

M.Mano, C.R.Kime, "Logic and Computer Design Fundamentals", Prentice Hall, latest edition.

REFERENCE BOOKS

- M. Mano, "Computer System Architecture", Englewood Cliffs, NY: Prentice Hall, latest edition.
- Patterson, D.A., and Hennessy J. L., "Computer Organization and Design: The Hardware/Software Interface", Morgan Kaufmann, latest edition.

COURSE AIM

The course introduces the student to the principles of design, build and test of special-purpose processors. Moreover, the students are introduced to the concepts of evaluating the performance of such processors. It is intended for the final year BS. Students or first year graduates specializing in computer engineering

COURSE OBJECTIVES

The course introduces the student to the principles of design, build and test of special-purpose processors. Moreover, the students are introduced to the concepts of evaluating the performance of such processors. It is intended for the final year BS. Students or first year graduates specializing in computer engineering.

COURSE OUTLINE

Week Number 1: Introduction to ISA-based Computer Design, Sequencing and Control.

Week Number 2: Hardwired and Micro-Programmed Control.

Week Number 3: Single-Cycle Hardwired Control and Multiple-Cycle Micro-Programmed Control.

Week Number 4: Pipelined Control and Performance Evaluation.

Week Number 5: Instruction Set Architecture and Addressing Evaluation.

Week Number 6: Central Processing Unit Design.

Week Number 7: 7th week exam.

Week Number 8: High Performance CPU Concepts.

Week Number 9: Design Parameters; Area, Time and Cost.

Week Number 10: Operational Analysis.

Week Number 11: M/G/I Queuing model.

Week Number 12: 12th Week Exam.

Week Number 13: Discrete-Time Markov Chains.

Week Number 14: Benchmark System Evaluation.

Week Number 15: Revision

Week Number 16: Final Exam.