COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Electronics and Communications Engineering, Cairo

Graduation Project Description Form

Project Supervisor(s): Dr. Hesham Nabil Mohamed

Project Title: A Concurrent Dual-Band Low Noise Amplifier for Modern Wireless Applications

Duration from mo/year 9/2013 till mo/year 7/2014

Product Category

Algorithm____ Hardware____ Software ✓

Standards:

Safety: UL, CE______ IEEE ______ FCC__

Other ✓

Practical Realization Form

PCB ______ Firmware___ Embedded CPU Kit (ARM, ..etc):____________

PC Software ______ Ready-made Package_____ DSP Kit____ FPGA Kit__

VLSI Schematics ✓ VLSI Layout _ VLSI Silicon (ASIC) ✓

Language

VHDL/Verilog______ Matlab ______ C/C++/Java ______

Graduation Project Description Form

Productization

Finished Product Form:____ Possible Commercialization ______

Amount of funds needed for buying components: ______

IEEE GOLD Made-In-Egypt/Engineering Day: __

ITAC (ITIDA) or NTRA Funding Application:____

Testing

Functional___ Simulation✓ Parameters__ Final Hardware_____Other:

Lab Test Setup

EMC ______ Environmental Microwave _______ Analog Lab_ Other:

CAD Tools *(No unauthentic software is allowed):*

Advanced Design System/Cadence Analog Design Environment

Elective Classes Required:

Radio Frequency Integrated Circuit Design

COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Electronics and Communications Engineering, Cairo

Graduation Project Description Form

Abstract

STANDARD receiver architectures, such as superheterodyne and direct conversion, accomplish high selectivity and sensitivity by narrow-band operation at a single input frequency. These modes of operation limit the system's available bandwidth and robustness to channel variations and thus its functionality. On the other hand, wide-band modes of operation are more sensitive to out-of-band unwanted signals (blockers) due to transistor nonlinearity. These out-of-band blockers can severely degrade receiver's sensitivity. The diverse range of modern wireless applications necessitates communication systems with more bandwidth and flexibility.

More recently, dual-band transceivers have been introduced to increase the functionality of such communication systems by switching between two different bands to receive one band at a time. While switching between bands improves the receiver's versatility (e.g., in multiband cellular phones), it is not sufficient in the case of a multi functionality transceiver where more than one band needs to be received simultaneously (e.g., a multiband cellular phone with a global positioning system, global position system (GPS), receiver and a Bluetooth interface). Using conventional receiver architectures, simultaneous operation at different frequency bands can only be achieved by building multiple independent signal paths with an inevitable increase in the cost, footprint, and power dissipation. Although there have been efforts to minimize the number of additional components used for the second band of operation (e.g., for adding GPS to a CDMA phone), none of these efforts attempt simultaneous reception of more than one band.

In this project, a concurrent dual-band receiver architecture is introduced that is capable of simultaneous operation at two-different frequencies without dissipating twice as much power or a significant increase in cost and footprint. This concurrent operation can be used to extend the available bandwidth, provide new functionality, and/or add diversity to battle channel fading. Concurrent operation is realized through an elaborate frequency conversion scheme in conjunction with a concurrent dual-band low-noise amplifier (LNA). These concurrent multiband LNAs provide simultaneous narrow-band input matching and gain at multiple frequency bands, while maintaining low noise.

Graduation Project Description Form

Project Steps of Implementation:

1. Study of main architectures of RF receivers
2. Study of current advances of single-band LNAs from technological and architectural points of view.
3. Understanding the general design methodology of concurrent multiband LNAs
4. Understanding ADS/Cadence design environment
5. Dual LNA Initial design calculations. Design, simulation and optimization using ADS/virtuso CAD tool.
6. Layout, of the proposed design
7. Design Rule Check DRC, Layout versus Schematic LVS, Parasitic Extraction PEX of the design.
8. Post layout simulations and verification of the design.

References and Links