COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Electronics and Communications Engineering, Cairo

Graduation Project Description Form

Project Supervisor(s): Dr. Hesham Nabil Mohamed

Project Title: Design of a low noise CMOS Instrumentation Amplifier for sensor applications

Duration from mo/year 9/2013 till mo/year 7/2014

Product Category

Algorithm____ Hardware____ Software ✓

Standards:

Safety: UL, CE_____ IEEE _____ FCC__

Other ✓

Practical Realization Form

PCB _____ Firmware___ Embedded CPU Kit (ARM, ..etc):_____

PC Software _____ Ready-made Package_____ DSP Kit___ FPGA Kit__

VLSI Schematics ___ VLSI Layout _____ VLSI Silicon (ASIC) ✓

Language

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VHDL/Verilog_____ Matlab _____ C/C++/Java _____

Productization

Finished Product Form:____ Possible Commercialization _____

Amount of funds needed for buying components: _____

IEEE GOLD Made-In-Egypt/Engineering Day: ___

ITAC (ITIDA) or NTRA Funding Application:____

Testing

Functional___ Simulation✓ Parameters___ Final Hardware_____Other:

Lab Test Setup

EMC _____ Environmental_ Microwave _____ Analog Lab_ Other:

CAD Tools *(No unauthentic software is allowed):*

Cadence Analog Design Environment

Elective Classes Required:

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Analog VLSI Circuit Design

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Abstract

Usually, a sensor output is a very weak signal within a noisy environment. A low noise instrumentation amplifier is often needed to extract the signal from such a noisy environment & provide a clean amplified replica. In this project, a fully differential CMOS instrumentation amplifier IA will be designed, using Cadence Integrated Circuit design tool based on a 0.13µm fabrication process. The IA will be specified to meet several design specifications over process variations that include slow-slow, slow-fast, fast-slow, and fast-fast for PMOS and NMOS transistors. A folded cascode stage with an NMOS driven common source amplifier output stage will be adopted to meet the required specifications

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Project Steps of Implementation:

1. Study of various instrumentation amplifier topologies
2. Study of different low noise techniques
3. Understanding Cadence design environment
4. IA Design: Initial design calculations. Design, simulation and optimization using virtuso CAD tool.
5. Layout, of the proposed design
6. Design Rule Check DRC, Layout versus Schematic LVS, Parasitic Extraction PEX of the design.
7. Post layout simulations and verification of the design.

References and Links