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VLSI Design and Layout of Down-Converter IC for I-Q Zero-IF Demodulators used in 3.5G/LTE/WiMAX Receivers

Modern communications receivers used in 3.5G, LTE, WiMAX, and Software Defined Radios (SDRs) use Direct I-Q quadrature down-conversion (zero-IF), followed by analog-to-digital conversion.

This project is a VLSI re-design of an IC which combines the properties of real-life ICs used in 3.5G communication systems. The basic functional units are

(1) A balanced I-Q mixer circuit close to the commercial IC "TRF371109" (http://www.ti.com/lit/ds/slws172a/slws172a.pdf)

(2) A High speed Analog to Digital (A/D) Converters resembling ADS62P42 (http://www.ti.com/lit/gpn/ads62p42).

In this project, the students will design a balanced RF mixer, followed by high speed A/D converter using the latest transistor technology. The project will go through all phases from system requirements specifications, circuit design, VLSI layout, and post layout circuit simulation. The whole flow will be implemented using opensource design and layout tools and simulators.