



COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Electronics and Communications Engineering, Cairo

Graduation Project Description Form

Project Supervisor(s): Prof. Khaled Shehata

Project Title: Design and implementation of DVB-S2 Module

Generation Cellular Networks.

Duration from 9/2013 ___till 7/2014 _____

Product Category

Algorithm___ Hardware✓___ Software✓___

Standards:

Safety: UL, CE_____ IEEE ✓___ FCC___

Other _____

Practical Realization Form

PCB _____ Firmware___ Embedded CPU Kit (ARM, ..etc):_____

PC Software _____ Ready-made Package___ DSP Kit___ FPGA Kit_✓

VLSI Schematics ___ VLSI Layout ___ VLSI Silicon (ASIC)_____

Language



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VHDL/Verilog Matlab C/C++/Java _____

Productization

Finished Product Form: _____ Possible Commercialization _____

Amount of funds needed for buying components: _____

IEEE GOLD Made-In-Egypt/Engineering Day: _

ITAC (ITIDA) or NTRA Funding Application: _

Testing

Functional Simulation _____ Parameters _____ Final Hardware Other: _____

Lab Test Setup

EMC _____ Environmental _____ Microwave _____ Analog Lab _____

Other: _____

CAD Tools *(No unauthentic software is allowed):*

Elective Classes Required:



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EC 535 Digital VLSI Design



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Abstract

Nowadays, digital satellite TV is the most popular system which provides a global delivery of digital television and data services through satellite. The digital video broadcasting DVB-S2 is the second generation system for satellite TV to make use of the improvements that have emerged since the publication of the DVB-S. DVB-S2 is a single, very flexible standard covering a variety of applications by satellite. Using innovative and more efficient channel coding methods and higher order modulation modes enable DVB-S2 works with higher efficiency than DVB-S. DVB-S2 has been optimized for digital multi-program television broadcasting services and high definition television (HDTV) broadcasting services to be used for primary and secondary distribution in the fixed satellite service (FSS) and the broadcasting satellite service (BSS) bands.

The aim of this project is to design and implement a DVB-S2 module on an FPGA using VHDL design entry.



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References and Links