



University/Academy: Arab Academy for Science, Technology & Maritime Transport
Faculty/Institute: College of Engineering & Technology
Program: B.Sc Computer Engineering

Form no. (12): Course Specification

1- Course Data

Course Code: CC317	Course Title: Digital Systems Design	Academic Year/Level: year 3 / semester 5
Specialization: Computer Engineering	Credit Hours: 3 Lecture: 2 Tutorial: 2 Lab: 2	Prerequisite ----- CC216

2- Course Aim

To introduce the students to combinational and sequential digital systems design and troubleshooting. The student will be able to implement their designs on FPGA/CPLD boards and handle interfacing problems.

3- Intended Learning Outcomes

a- Knowledge and Understanding	<p>a5. Engineering principles in the fields of logic design, circuit analysis, machine and assembly languages, computer organization and architectures, memory hierarchy, advanced computer architectures, embedded systems, signal processing, operating systems, real-time systems and reliability analysis.</p> <ul style="list-style-type: none"> • Identify codes, Standard Representation of logic Functions. • Tabulate Quine-McCluskey Algorithm • Define the design model using ASM charts • Describe propagation delay, Clock Skew, Timing Hazards • Demonstrate internal structure of the programmable chips and the differences between the various architectures. • Interpret VHDL or Verilog Principles. • Associate the ASM charts using combinational and sequential logic • Examine the FPGA boards and the possible interface and the design of these interfaces. • Distinguish between a hierarchical design model, modular design and generic design • Collect case- Studies and Applications with VHDL-based design using FPGA, CPLD
b- Intellectual Skills	<p>b2. Think in a creative and innovative way in problem solving and design using the latest technologies and solve engineering problems, often on the basis of limited and possibly contradicting information while identifying symptoms in problematic situations.</p> <ul style="list-style-type: none"> • Change each step of the design idea into an ASM block. • Calculate the propagation delay and detect any clock skew and/or timing hazards. • Discover the purpose of each of the possible interface • Acquire presentation Skills • Determine sharing pitfalls and fallacies
c- Professional Skills	<p>c2. Create and/or re-design a process, component or system, and carry out specialized engineering designs with neatness and aesthetics in design and approach.</p> <ul style="list-style-type: none"> • Integrate the interface designs into the original digital system. • Design hierarchical, modular, and generic design . • Design a C++ or Java program that implements Quine-McCluskey. • Transform the resulting ASM chart into a digital logic design using standard steps. <p>c3. Use computational facilities and techniques, measuring instruments, workshops and laboratory equipment, wide range of analytical tools, techniques, and software</p>

	<p>packages pertaining to the computer engineering to design experiments, collect, analyze and interpret results and develop required computer programs.</p> <ul style="list-style-type: none"> • Use the Xilinx CAD tools to design combinational circuits using VHDL or Verilog • Implement the combinational and sequential design using VHDL or Verilog on the Xilinx CAD tool • Classify sharing technical difficulties
d- General Skills	<p>d2. Work in stressful environment and within constraints, communicate effectively, lead and motivate individuals and effectively manage tasks, time, and resources.</p> <ul style="list-style-type: none"> • Verify theory with practice • Master VHDL or Verilog hardware description language. • Familiarize with the FPGA and CPLD boards available in the lab.

4- Course Content

Week No.1	Introduction to digital design
Week No.2	Quine-McCluskey Simplification Algorithm
Week No.3	Algorithmic state machine (ASM) chart
Week No.4	Timing Analysis of Digital Designs
Week No.5	Physical Layout of PLA, PLD, CPLD, GAL, and FPGA
Week No.6	Combinational logic design practices: VHDL
Week No.7	7 th Week Exam + Sequential logic design practices
Week No.8	Sequential logic design practices
Week No.9	Interfacing with FPGA/CPLD boards
Week No.10	Interfacing with FPGA/CPLD boards
Week No.11	Hierarchical and Modular Design
Week No.12	12 th Week Exam + Hierarchical and Modular Design
Week No.13	Project Ideas
Week No.14	Project Discussions
Week No.15	Revision
Week No.16	Final Exam

5- Teaching and Learning Methods

<ul style="list-style-type: none"> • Lectures • Tutorials • Reports & sheets • Laboratories • Seminars

6-Teaching and Learning Methods for Students with Special Needs

<ul style="list-style-type: none"> • Lectures • Tutorials • Reports & sheets • Laboratories • Seminars <p>The academic advisors of each student, as well as dedicated department TAs monitor the students' progress and solve any problem he/she may encounter.</p>
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7- Student Assessment

a-Procedures used	<p>1-Written Examinations to assess The Intended Learning Outcomes.</p> <p>2-Class Activities (Reports, Discussions, -----) to assess The Intellectual Skills.</p>								
b- Schedule:	<table> <tr> <td>Assessment 1</td> <td>7th Week Written Exam</td> </tr> <tr> <td>Assessment 2</td> <td>12th Week Written Exam</td> </tr> <tr> <td>Assessment 3</td> <td>Continuous Assessments</td> </tr> <tr> <td>Assessment 4</td> <td>16th Week Final Written Exam</td> </tr> </table>	Assessment 1	7 th Week Written Exam	Assessment 2	12 th Week Written Exam	Assessment 3	Continuous Assessments	Assessment 4	16 th Week Final Written Exam
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c- Weighing of Assessment	7 th Week Examination	30 %
	12 th Week Examination	20 %
	Final-term Examination	40 %
	Oral Examination	0 %
	Practical Examination	0 %
	Semester Work	10 %
	Total	100%

8- List of References:

a- Course Notes	Available on the moodle http://lms.aastmt.org
b- Required Books (Textbooks)	Wakerly, John F, "Digital Design: Principles and Practice (1374)", Pearson Education 4ED
c- Recommended Books	<ul style="list-style-type: none"> • Logic and Computer Design Fundamentals , Mano and Kime , Fourth Edition , Prentice Hall , 2007. • F. P. Processor, D. E. Wiskel, "The art of digital Design and introduction to top-Down Design", 2nd Ed., Prentice hall, 1997 • Fundamentals of Digital Logic with VHDL Design, Stephen Brown and Zvonko Vranesic, McGraw-Hill, 3rd edition, 2008.
d- Periodicals, Web Sites, etc.	N/A

Course Instructor:
Dr. Hala Farouk

Program Manager:
Prof. Dr. Mohamad AbouEI-Nasr

Dean of College of Engineering and Technology of AASTMT
Name: **Prof. Moustafa Hussein Aly**
Signature:

Executive Manager of Quality Assurance Center of AASTMT
Name: **Prof. Aziz Ezzat**
Signature: