COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Electronics and Communications Engineering

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Course Title: Electronic Devices I

Course Code: EC 233

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Sheet 7

I. Indicate whether each of the following statements is true or false *(give reasons)*:

1- At thermal equilibrium, the total current through a pn junction is zero because the electron current is balanced by the hole current.

2- The built-in potential increases as the doping on both sides of the junction are increased.

3- The cut-in voltage of diode made of low energy gap semiconductor is higher than that of a diode made of high energy gap semiconductor.

4- As the temperature is increased, the built-in potential is decreased.

5- The space-charge (depletion) layer width increases with doping.

6- The electric field in the depletion layer of a pn junction at equilibrium is directed from the n-side to the p-side.

7- As the temperature is lowered, the built-in voltage decreases.

8- For a pn-junction diode at a fixed temperature, the higher is the potential barrier (built-in potential), the lower is the depletion layer width.

II. Choose the correct answer justifying your choice:

1- The built-in potential in a pn junction prevents……. ……
(a) more holes to diffuse from n-side to p-side
(b) more electrons to diffuse from p-side to n-side
(c) more electrons to move from the valence band to the conduction band
(d) more electrons to diffuse from n-side to p-side

2- The electric field in the depletion layer of a pn junction of has an aboslute maximum value at …….
(a) the p-neutral region (b) the n-neutral region
(c) the metallurgical junction (d) the point of highest potential

3- For a pn junction at thermal equilibrium, The electric potential is highest ……
(a) in the p-neutral region (b) in the n-neutral region
(c) at the metallurgical junction (d) at the point of maximum electric field

III.Solve the following problems:

1- Consider an abrupt silicon pn junction in which the acceptor concentration is 4×10^{18} cm^{-3} and the donor concentration is 10^{16} cm^{-3}. Determine the depletion widths for the junction and the maximum electric field at room temperature (300 K) where the relative permitivity of silicon 11.8.

2- Figure (1) presents an energy band diagram of an abrupt silicon pn junction. Let the sample be maintained at 300 K and $N_a = 5x10^{15}cm^{-3}$. Use the cited energy band diagram to answer the following three parts:

i- What is the bias condition of the diode? Justify
ii- Calculate the ration x_p/w .
iii- Find the doping concentration N_D at in the $x > x_n$ region.

3- A Si p-n junction has the following : $N_D = 4x10^{24}$ m^{-3} in the n-side , $N_A=2x10^{22}$ m^{-3} in the p-side . Calculate the built-in junction voltage and the maximum electric field within the depletion region.

4- A Si^+ p-n 10 cm^2 in area has N_D 10^{15} cm^{-3} in the n-side. Draw the energy band diagram in the thermal equilibrium condition of such junction indicate the following on it after calculation.
a- $(E_{fn}-E_i)$ in ev.
b- qV_{bi} if $E_i-E_{fp} = 0.5$ eV

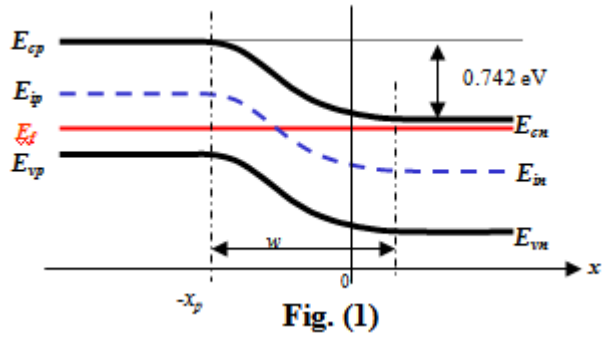

Fig. (1)

This work had been prepared with the help of Dr. Wael Fikry and Dr. Tarek Abd El_Kader.

Good Luck ☺