

Arab Academy For Science & Technology & Maritime Transport College of  
Engineering & Technology

EC332: Electronic Devices (2).



SHEET (4)

[1] Consider the circuit shown of the figure 1,  $I_{DQ1}$  of  $80 \mu\text{A}$ ,  $V_t = 0.6\text{V}$ ,  $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$ ,  $L = 0.8 \mu\text{m}$  and  $W = 4 \mu\text{m}$ , the drain voltage of  $Q_1$  designed to be  $1\text{V}$  and applied to the gate of  $Q_2$ , assume the two transistors are identical (Assume  $\lambda = 0$ ).

Find:

- The drain current of  $Q_2$ .
- The drain voltage of  $Q_2$ .

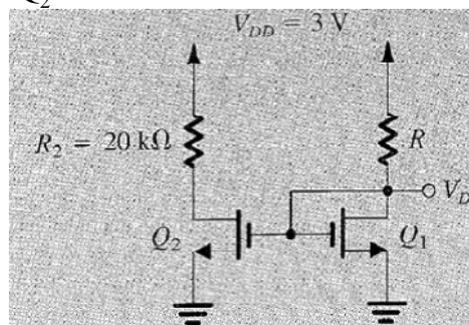


Figure 1

[2] Using two transistors  $Q_1$  and  $Q_2$  having equal length but widths related by  $W_2/W_1 = 5$ , Design the circuit shown on figure 2 to obtain  $I = 0.5 \text{ mA}$ . Let  $V_{DD} = V_{SS} = 5$ ,  $(\mu_n C_{ox} W/L)_{Q1} = 0.8 \text{ mA}/\text{V}^2$ ,  $V_t = 1\text{V}$  and  $\lambda = 0$ .

- Find the required value for  $R$ .
- What is the voltage at the gates of  $Q_1$  and  $Q_2$ ?
- What is the lowest voltage allowed at the drain of  $Q_2$  while  $Q_2$  remains in the saturation region?

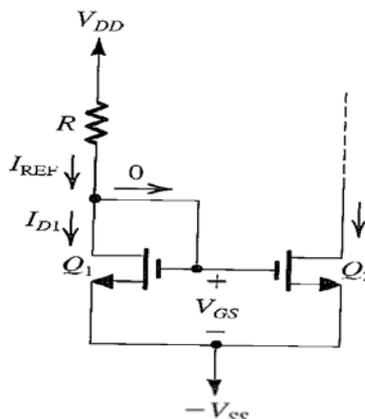


Figure 2

- [3] Consider the circuit shown in Figure 3. Using a 15v supply,  $V_t = 1.2 \text{ v}$ ,  $\lambda = 0$ ,  $K_n' = 80 \mu\text{A}/\text{V}^2$ ,  $W = 240 \mu\text{m}$  and  $L = 6 \mu\text{m}$ . Arrange that the drain current is 2 mA, with about one third of the supply voltage across  $R_S$  and  $R_D$ . Use 22 M $\Omega$  for the larger of  $R_{G1}$  and  $R_{G2}$ . What are the values of  $R_{G1}$ ,  $R_{G2}$ ,  $R_S$  and  $R_D$  that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of Saturation?

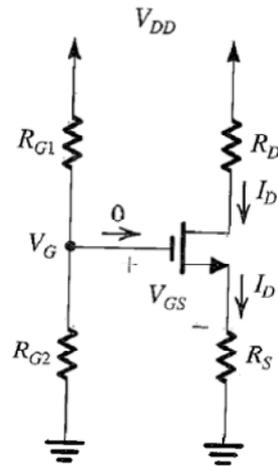


Figure 3

- [4] For the circuit shown in figure 4 with  $I = 1 \text{ mA}$ ,  $R_G = 0$ ,  $R_D = 5 \text{ k}$  and  $V_{DD} = 10 \text{ V}$ , consider the behavior in each following two cases. In each case, find the voltages  $V_S$ ,  $V_D$  and  $V_{DS}$  that results for each cases:
- $V_t = 1 \text{ V}$   $K_n' (W/L) = 0.5 \text{ mA}/\text{V}^2$
  - $V_t = 2 \text{ V}$   $K_n' (W/L) = 1.25 \text{ mA}/\text{V}^2$

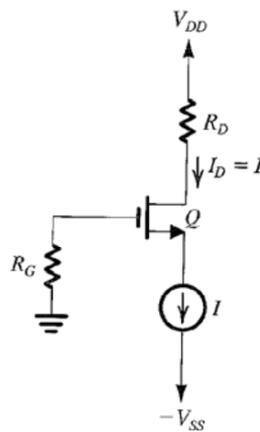


Figure 4

- [5] As shown in figure 6, using a 6V supply with an NMOS transistor for which  $V_t=1.2V$ ,  $K_n'(W/L)=3.2mA/V^2$  and  $\lambda=0$ , provide a design which biases the transistor at  $I_D=2mA$  with  $V_{DS}$  larger enough to allow saturation operation for a -2V negative signal swing at the drain. Use  $22M\Omega$  as the largest resistor in the feedback bias network. What values of  $R_D$ ,  $R_{G1}$  and  $R_{G2}$  have you chosen? Specify all resistors to two significant digits.

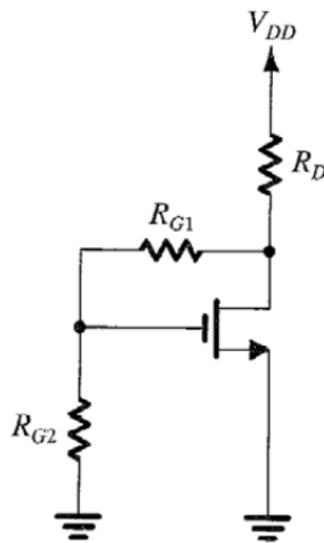


Figure 5