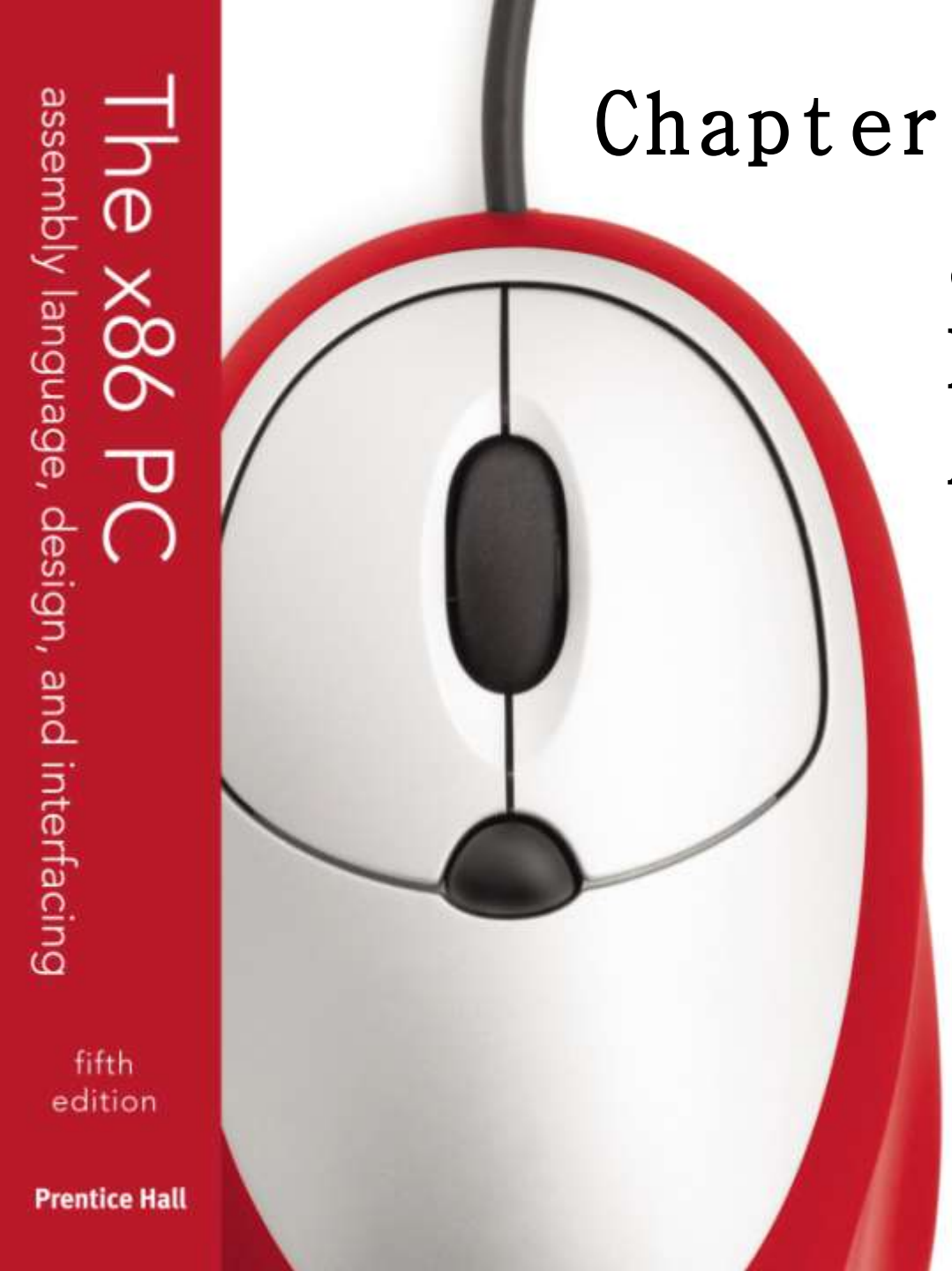

Chapter NINE

8088,80286 MICROPROCESSORS AND ISA BUS

The x86 PC

assembly language, design, and interfacing

fifth edition

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OBJECTIVES

this chapter enables the student to:

- State the function of the pins of the 8088.
- List the functions of the 8088 data, address, and control buses.
- State the differences in the 8088 microprocessor in maximum mode versus minimum mode.
- Describe the function of the 8284 clock generator chip and the 8288 bus controller chip.
- Explain the role of the 8088, 8284A, and 8288.
- Explain how bus arbitration between the CPU and DMA is accomplished.

9.1: 8088 MICROPROCESSOR
address bus

- 8088 has 20 address pins (**A0**–**A19**), allowing it to address a maximum of one megabyte of memory (2^{20} = 1M).
- To demultiplex address signals, a latch must be used to grab the addresses.

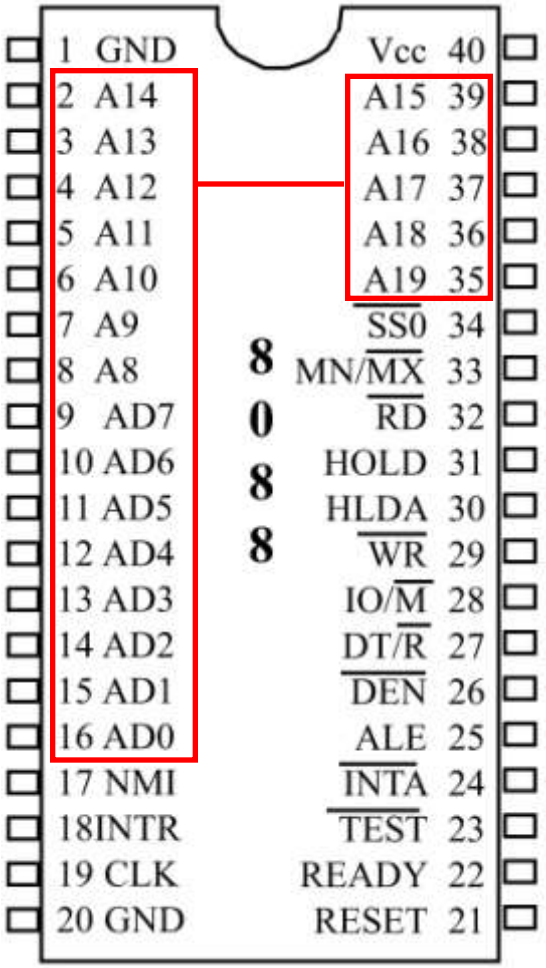


Fig. 9-1a 8088 in minimum mode

9.1: 8088 MICROPROCESSOR
data bus

- Due to chip packaging limitations in the 1970s, there was great effort to use the minimum number of pins for external connections.
  - Intel multiplexed address & data buses, using the same pins to carry two sets of information: address & data.
- Pins 9-16 (**AD0**–**AD7**) are used for both data and addresses in 8088.
  - **AD** stands for "address/data."
- The **ALE** (address latch enable) pin signals whether the information on pins AD0–AD7 is address or data.

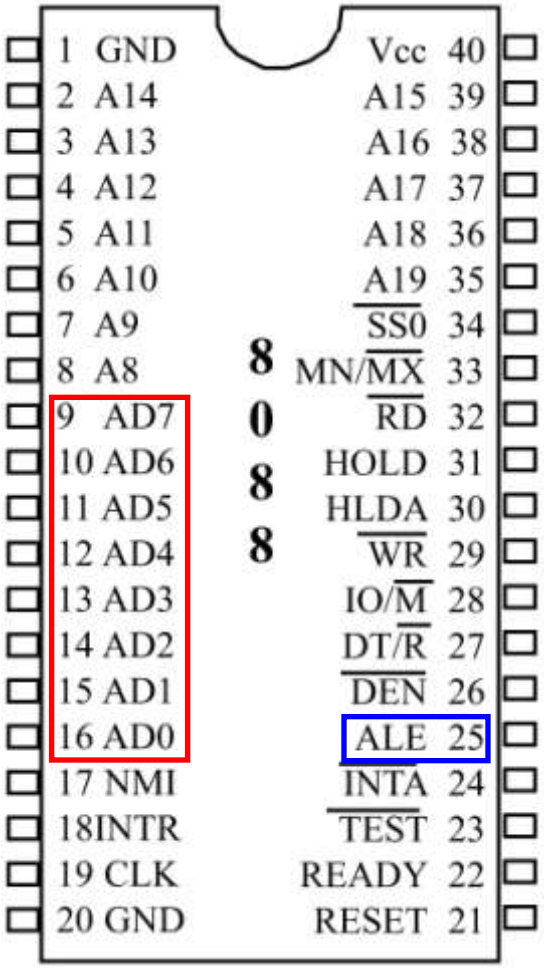


Fig. 9-1a 8088 in minimum mode

9.1: 8088 MICROPROCESSOR
data bus

- When 8088 sends out an address, it activates (sets *high*) the **ALE**, to indicate the information on pins **AD0**–**AD7** is the *address* (**A0**–**A7**).
  - This information must be *latched*, then pins AD0–AD7 are used to carry data.
- When data is to be sent out or in, **ALE** is low, which indicates that **AD0**–**AD7** will be used as *data* buses (**D0**–**D7**).
- The process of separating address and data from pins AD0–AD7 is called *demultiplexing*.

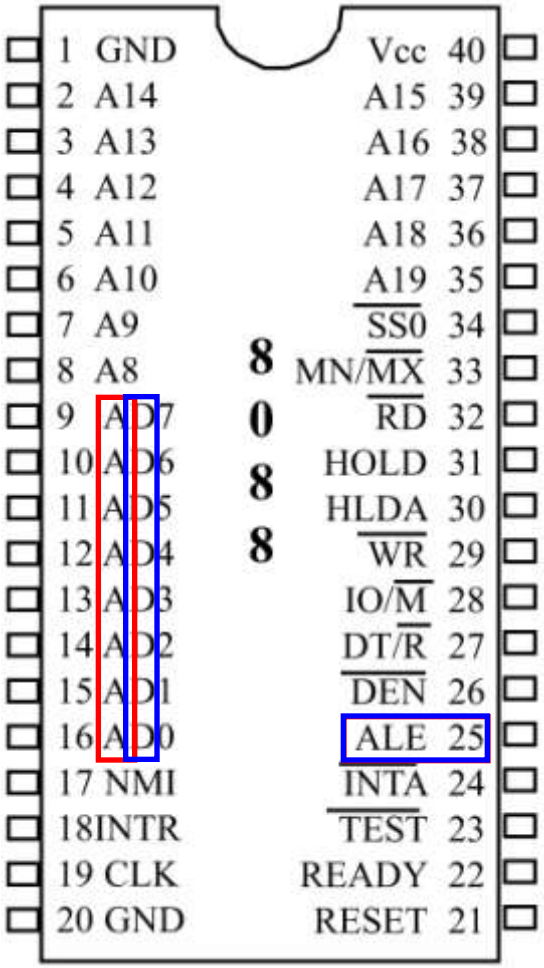


Fig. 9-1a 8088 in minimum mode

9.1: 8088 MICROPROCESSOR address bus

The most widely used latch is the 74LS373 IC.
Also used is the 74LS573, a 74LS373 variation.

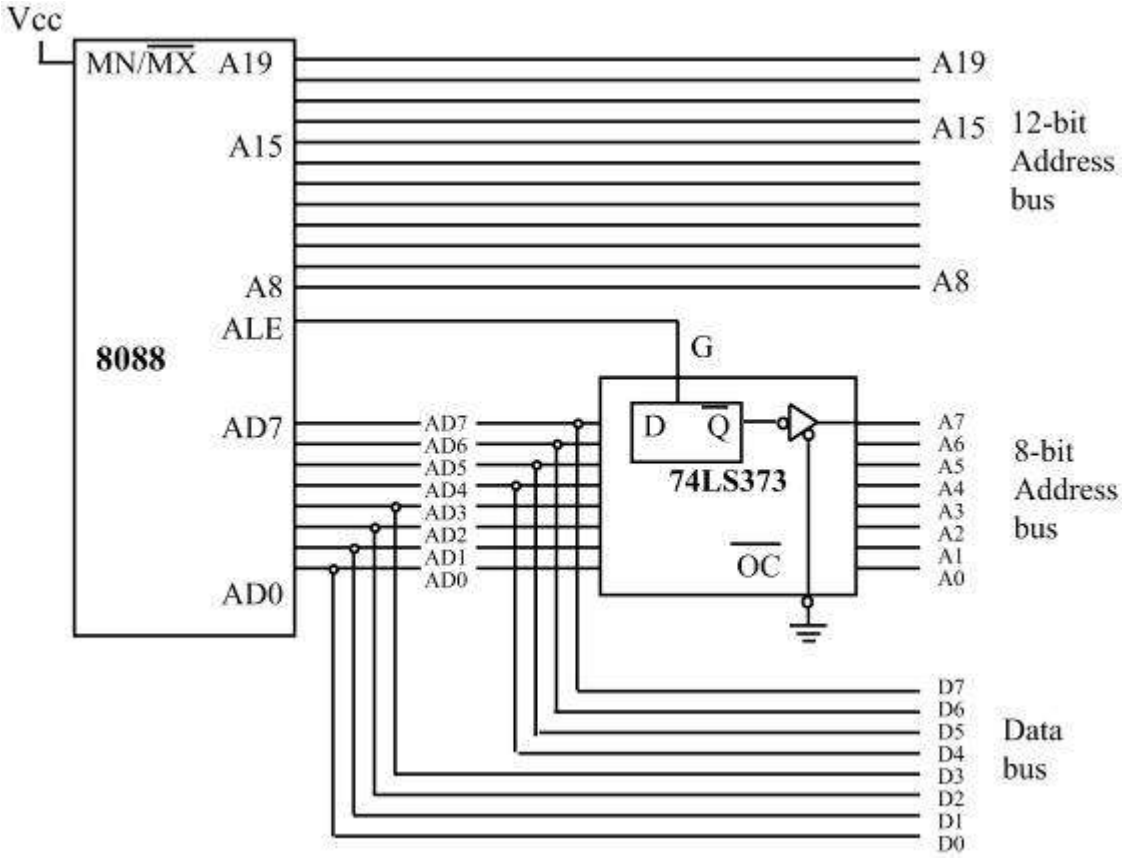
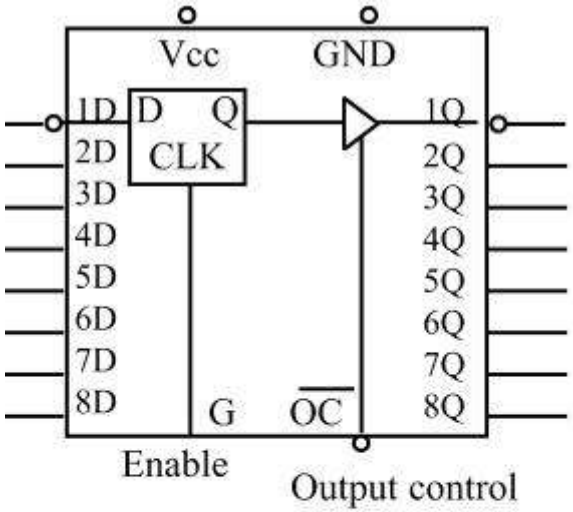


Fig. 9-2 Role of ALE in address/data demultiplexing



Function Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Fig. 9-3 74 LS373 D Latch

9.1: 8088 MICROPROCESSOR
control bus

- 8088 provides three pins for control signals:
  - RD, WR, and IO/$\overline{M}$.
    - RD & WR pins are both *active-low*.
    - IO/$\overline{M}$ is *low* for memory, *high* for I/O devices.

Four control signals are generated:
$\overline{IOR}$; **$\overline{IOW}$**;
$\overline{MEMR}$; **$\overline{MEMW}$**.

All of these signals must be active-low.

Table 9-1: Control Signal Generation

RD	WR	IO/M	Signal
0	1	0	$\overline{MEMR}$
1	0	0	$\overline{MEMW}$
0	1	1	$\overline{IOR}$
1	0	1	$\overline{IOW}$
0	0	x	Never happens

9.1: 8088 MICROPROCESSOR
control bus

- 8088 provides three pins for control signals:
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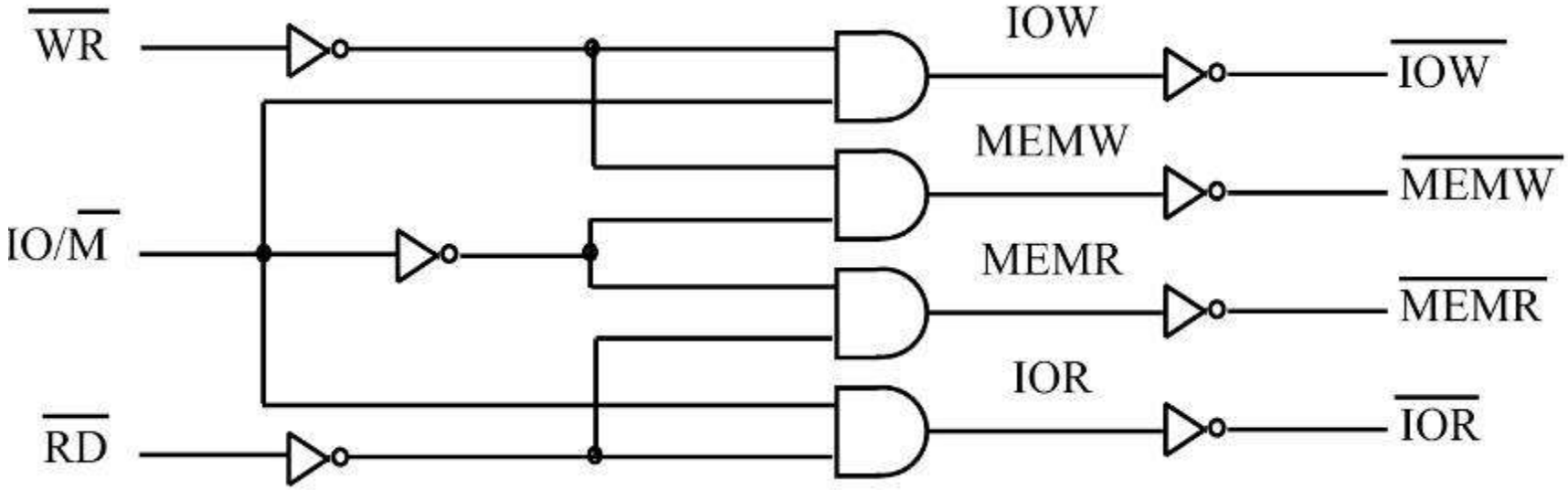
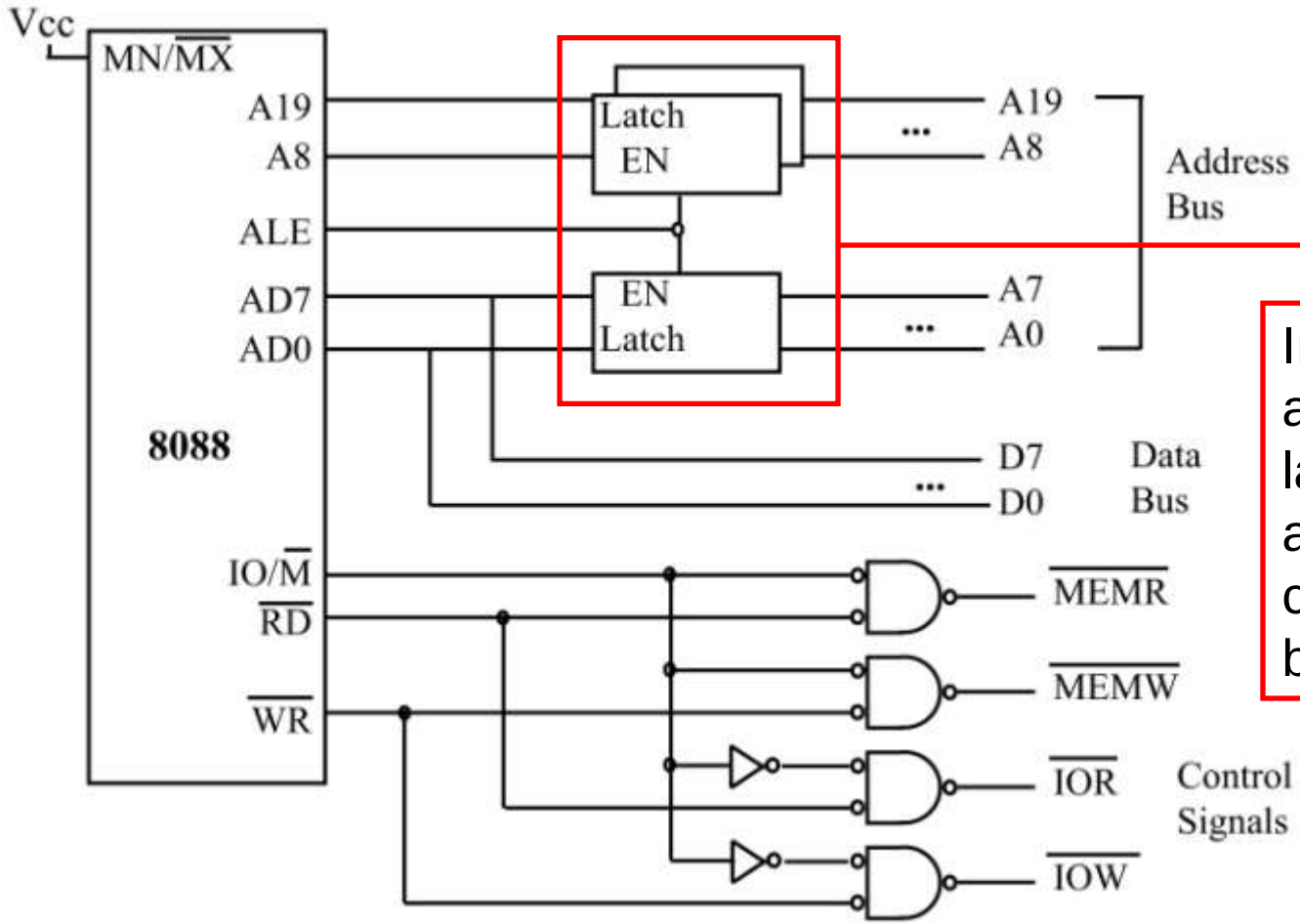


Fig. 9-4 Control signal generation

9.1: 8088 MICROPROCESSOR
address bus



In any system, all addresses must be latched to provide a stable, high-drive-capability address bus.

Fig. 9-5 Address,Data,and Control Buses in 8088-based System

9.1: 8088 MICROPROCESSOR
control bus

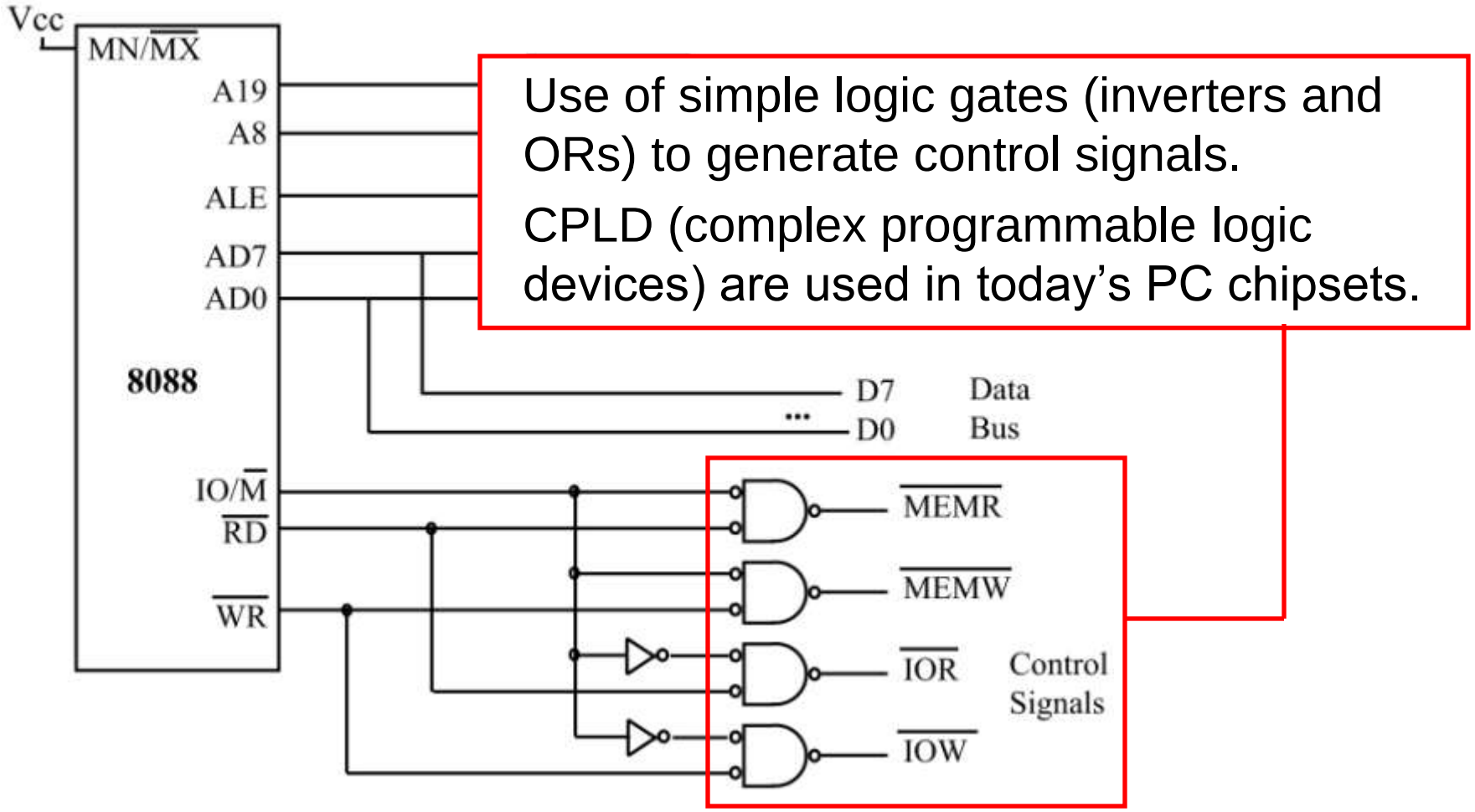


Fig. 9-5 Address,Data,and Control Buses in 8088-based System

9.1: 8088 MICROPROCESSOR
bus timing of the 8088

- 8088 uses 4 clocks for memory & I/O bus activities.
  - In read timing, **ALE** latches the address in the first clock cycle.
  - In the second and third cycles, the read signal is provided.
  - By the end of the fourth, data must be at the CPU pins.
  - The entire read or write cycle time is only 4 clock cycles.

If reading/writing takes more than 4 clocks, wait states (WS) can be requested from the CPU.

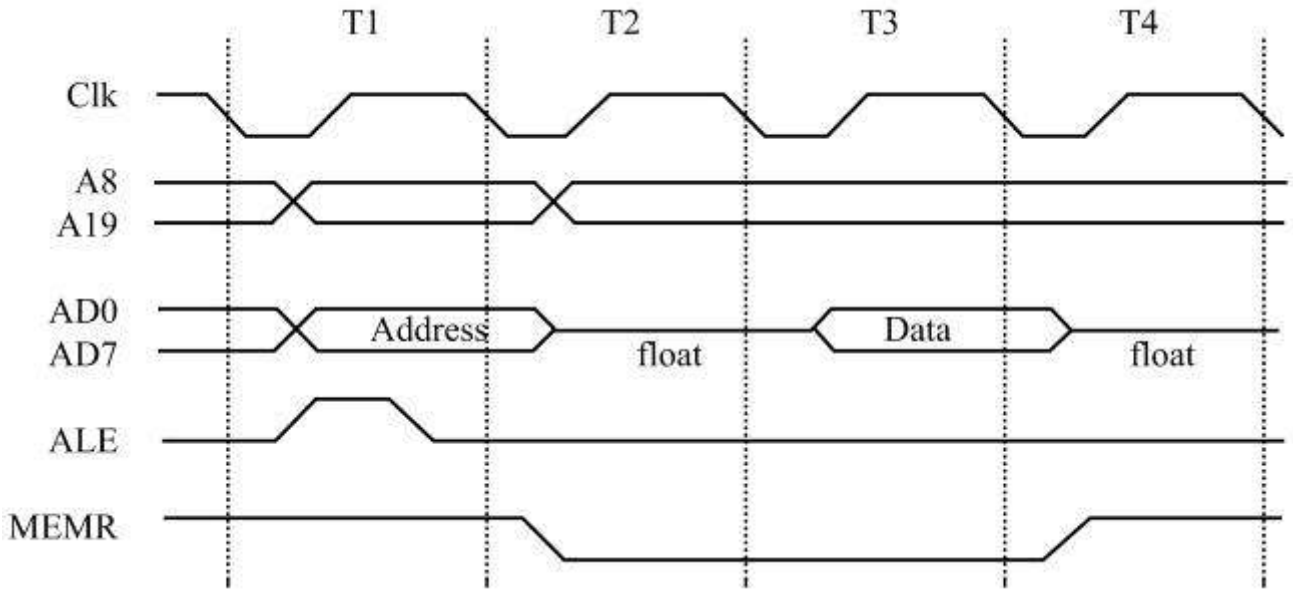


Fig. 9-6 ALE Timing

9.1: 8088 MICROPROCESSOR
other pins

- Pins 24–32 have different functions depending on whether 8088 is in minimum or maximum mode.
  - In maximum mode, 8088 needs supporting chips to generate the control signals.

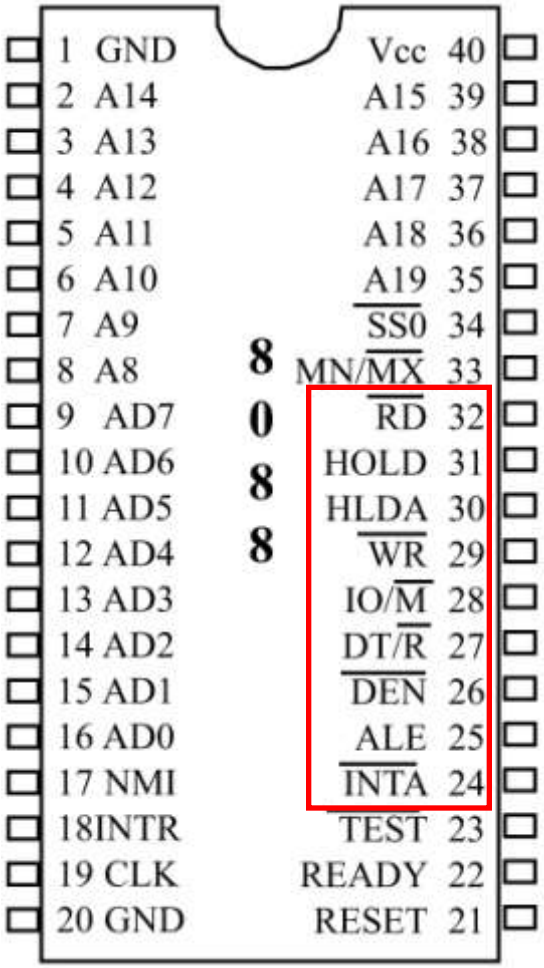


Fig. 9-1a 8088 in minimum mode

Functions of 8088 pins 24–32 in minimum mode.

Table 9-2: Pins 24–32 in Minimum Mode

Pin	Name and Function
24	INTA (interrupt acknowledge) Active-low output signal. Informs interrupt controller that an INTR has occurred and that the vector number is available on the lower 8 lines of the data bus.
25	ALE (address latch enable) Active-high output signal. Indicates that a valid address is available on the external address bus.
26	DEN (data enable) Active-low output signal. Enables the 74LS245. This allows isolation of the CPU from the system bus.
27	DT/R (data transmit/receive) Active-low output signal used to control the direction of data flow through the 74LS245 transceiver.
28	IO/M (input-output or memory) Indicates whether the address bus is accessing memory or an I/O device. In the 8088, it is low when accessing memory and high when accessing I/O. This pin is used along with RD and WR pins to generate the four control signals MEMR, MEMW, IOR, and IOW.

Functions of 8088 pins 24–32 in minimum mode.

Table 9-2: Pins 24–32 in Minimum Mode

Pin	Name and Function
29	WR (write) Active-low output signal. Indicates that the data on the data bus is being written to memory or an I/O device. Used along with signal IO/M (pin 28) to generate the MEMW and IOW control signals for write operations.
30	HLDA (hold acknowledge) Active-high output signal. After input on HOLD, the CPU responds with HLDA to signal that the DMA controller can use the buses.
31	HOLD (hold) Active-high input from the DMA controller that indicates that the device is requesting access to memory and I/O space and that the CPU should release control of the local buses.
32	RD (Read) Active-low output signal. Indicates that the data is being read (brought in) from memory or I/O to the CPU. Used along with signal IO/M (pin 28) to generate MEMR and IOR control signals for read operations.

9.1: 8088 MICROPROCESSOR
other pins

- **MN/MX** (minimum/maximum) - minimum mode is selected by connecting MN/MX (pin number 33) directly to +5 V.
  - Maximum mode is selected by grounding this pin.
- **NMI** (nonmaskable interrupt) - an edge-triggered (*low* to *high*) input signal to the processor that will make the microprocessor jump to the interrupt vector table after it finishes the current instruction.
  - Cannot be masked by software.
- **CLOCK** - an input signal, connected to the 8284 clock generator.

9.1: 8088 MICROPROCESSOR
other pins

- **INTR** (interrupt request) - an *active-high* level-triggered input signal continuously monitored by the microprocessor for an external interrupt.
  - This pin & INTA are connected to the 8259 interrupt controller chip.
- **READY** - an input signal, used to insert a wait state for slower memories and I/O.
  - It inserts wait states when it is *low*.
- **TEST** - in maximum mode, an input from the 8087 math coprocessor to coordinate communications.
  - Not used In minimum mode.

9.1: 8088 MICROPROCESSOR
other pins

- **RESET** - terminates present activities of the processor when a *high* is applied to the **RESET** input pin.

A presence of *high* will force the microprocessor to stop all activity and set the major registers to the values shown at right.

Table 9-3: IP and Segment Register Contents after Reset

Register	Contents
CS	FFFF
IP	0000
DS	0000
SS	0000
ES	0000

9.2: 8088 SUPPORTING CHIPS

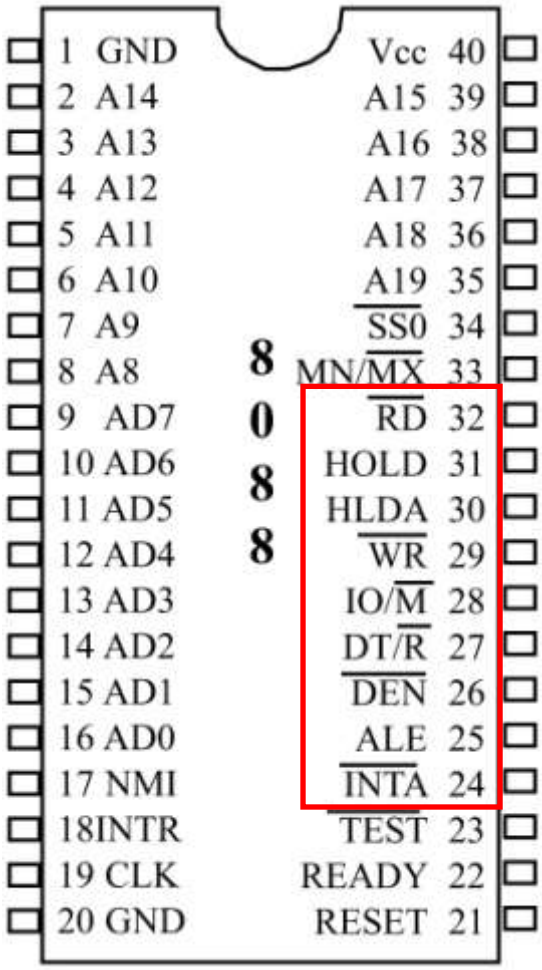


Fig. 9-1a 8088 in **minimum** mode

Comparing Fig. 9-1, 8088 in **minimum** mode, with Fig. 9-7, 8088 in **maximum** mode, shows that pins 24–32 have different functions.

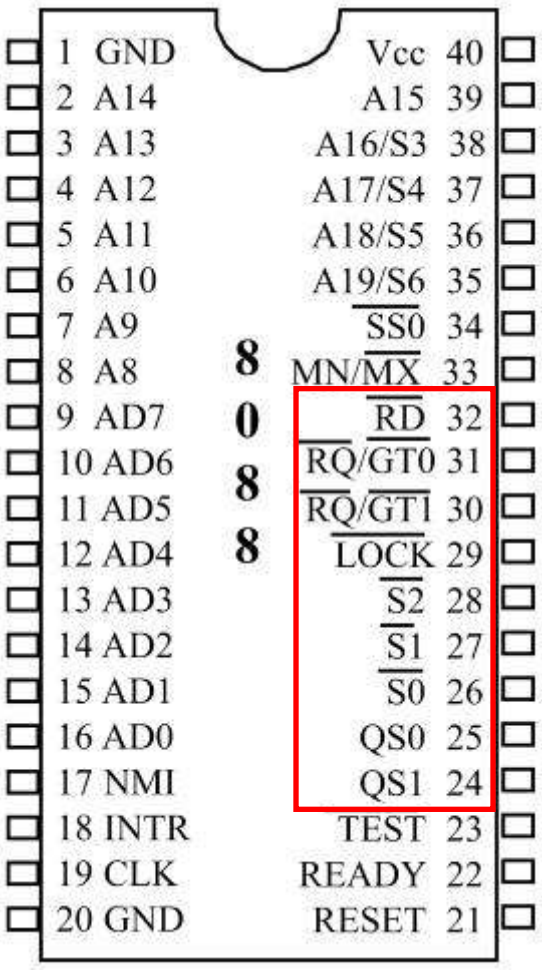


Fig. 9-7a 8088 in **maximum** mode

9.3: 8-BIT SECTION OF ISA BUS
local bus vs. system bus

An overview of the 8088 & supporting chips in the original PC.

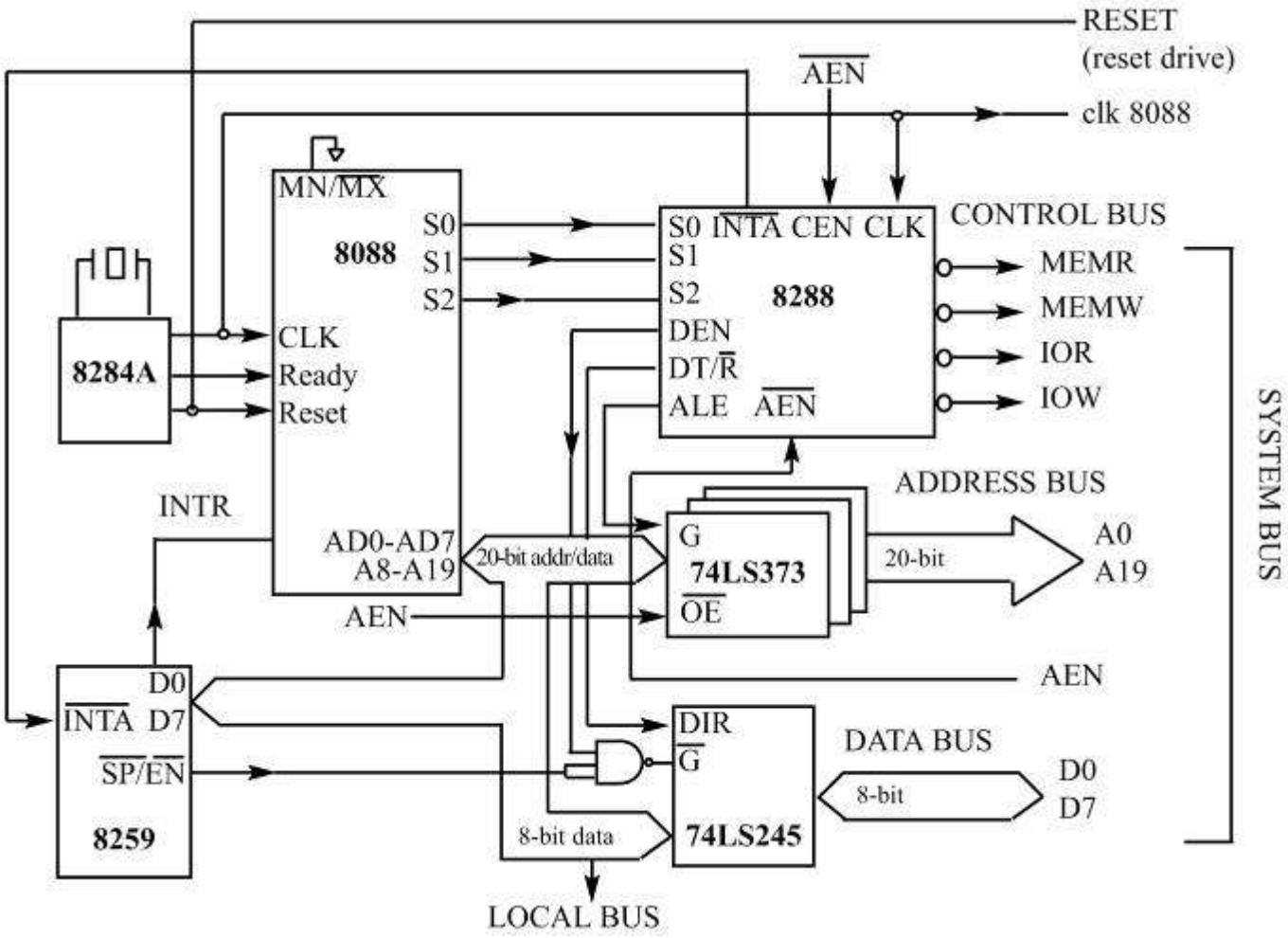
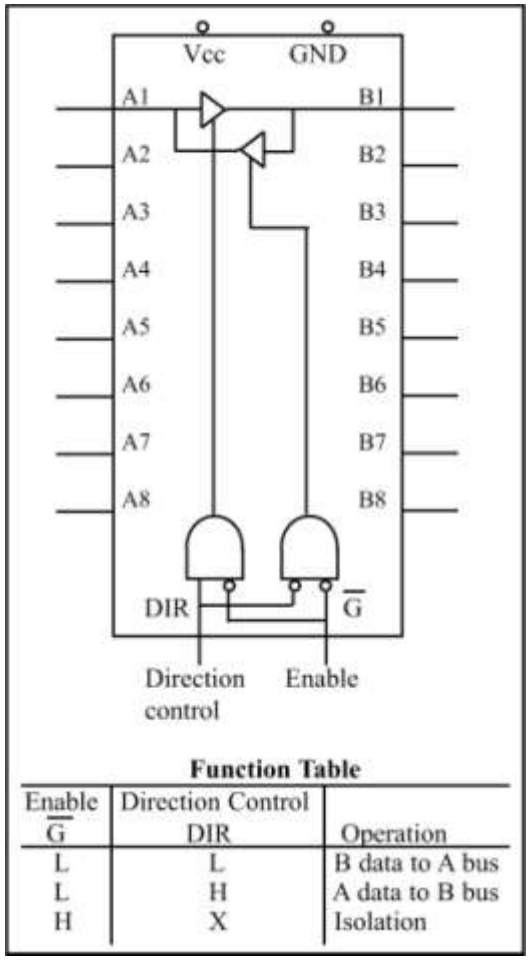


Fig. 9-11 8088 Connections and Buses in the PC/XT

9.3: 8-BIT SECTION OF ISA BUS
local bus vs. system bus

This diagram appears on page 238 of your textbook.

- Tri-state buffers isolate the local bus & system bus.
  - 74LS245 is a widely used chip for the data bus buffer since it is bidirectional.



Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

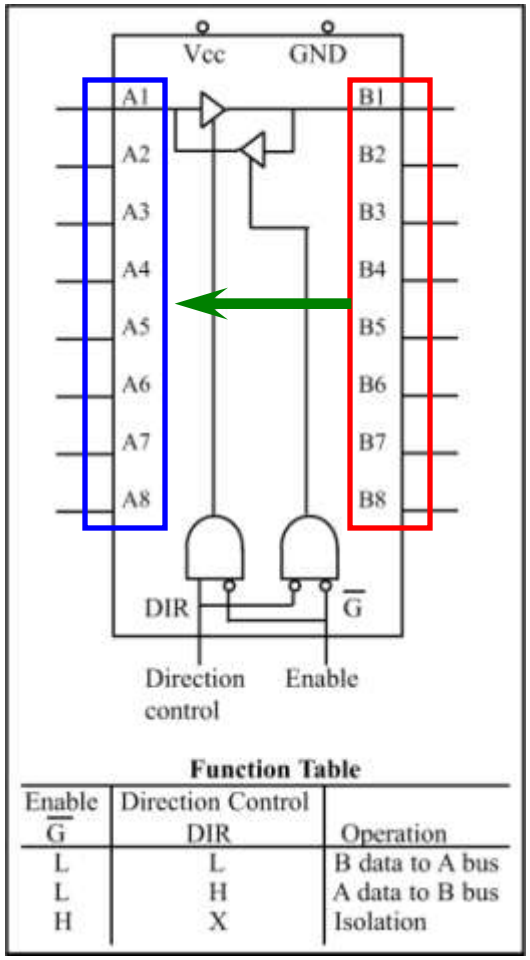
Fig. 9-10 74SL245 Bidirectional Buffer

9.3: 8-BIT SECTION OF ISA BUS
data bus

This diagram appears on page 238 of your textbook.

When **DT/$\overline{R}$** makes **DIR** ***low***, the information transfers *from* the **B** *to* the **A** side, taking information from the system data bus and bringing it to the 8088.

The bidirectional data bus goes through the 74LS245 transceiver.



Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
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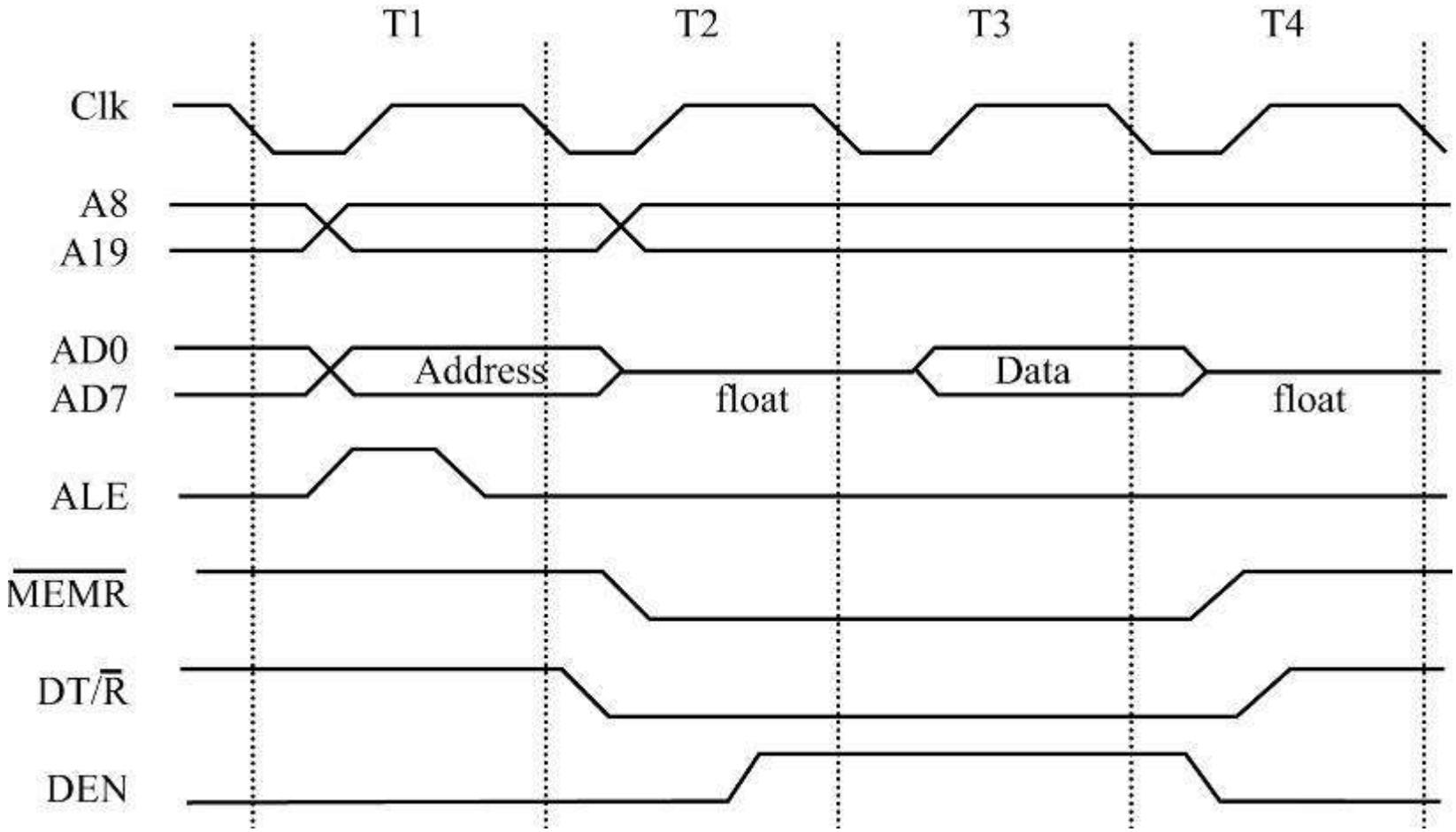
L	H	A data to B bus
H	X	Isolation

Fig. 9-10 74SL245 Bidirectional Buffer

9.3: 8-BIT SECTION OF ISA BUS
control bus

The timing for control bus activity.



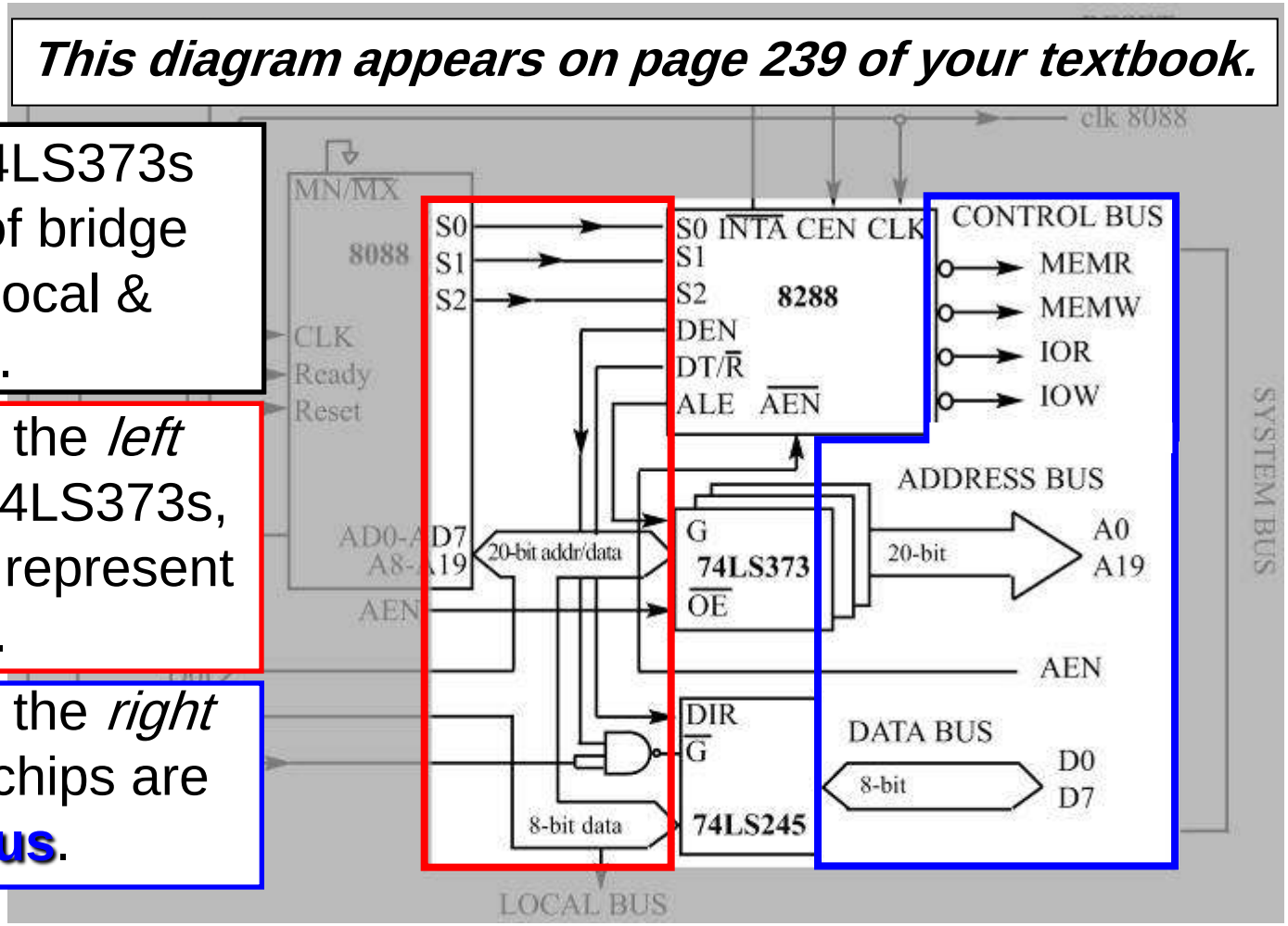
9.3: 8-BIT SECTION OF ISA BUS
local bus vs. system bus

This diagram appears on page 239 of your textbook.

74LS245 & 74LS373s play the role of bridge to isolate the local & system buses.

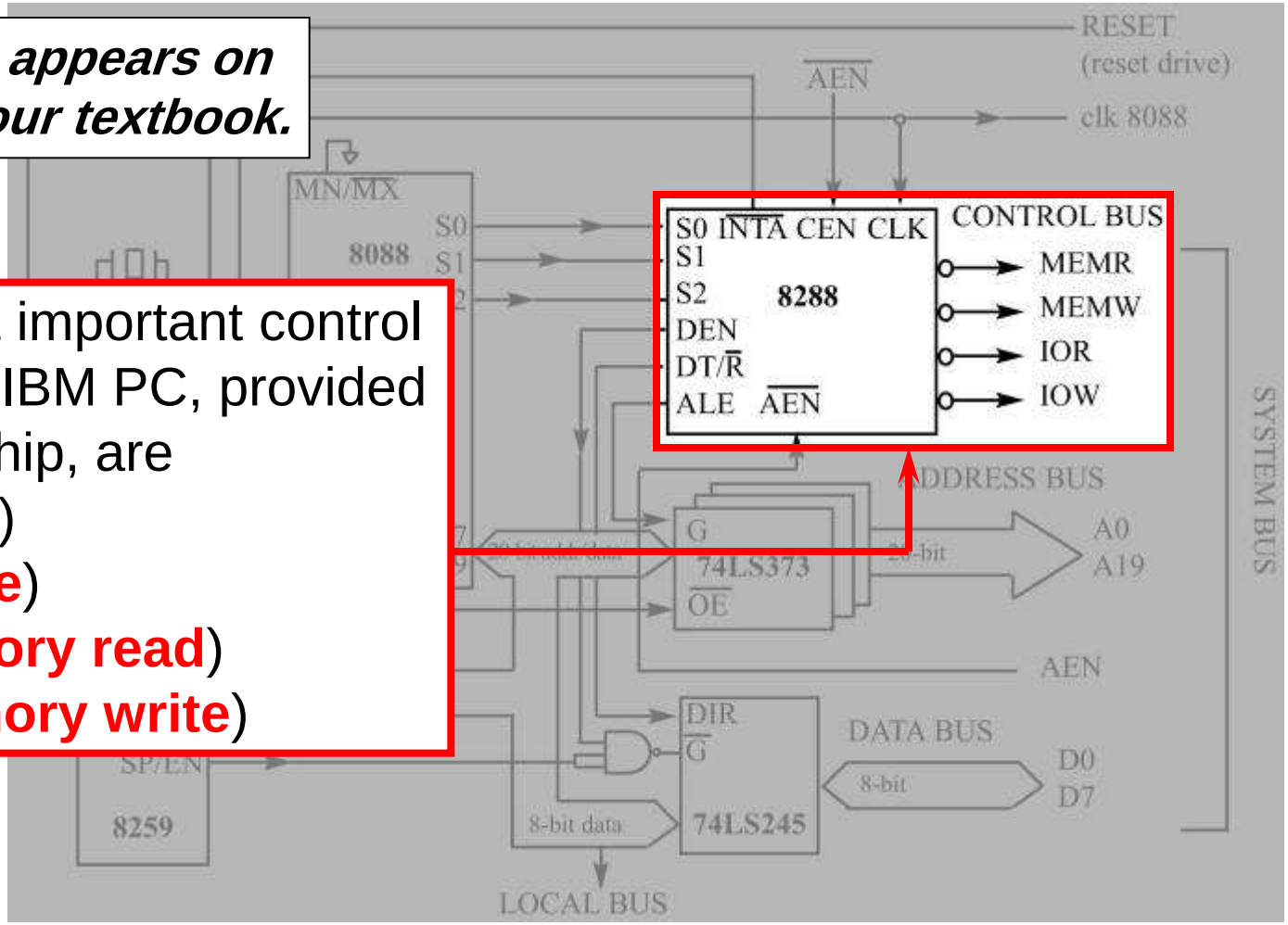
Everything on the *left* of the 8288, 74LS373s, and 74LS245 represent the **local bus**.

Everything on the *right* side of those chips are the **system bus**.



9.3: 8-BIT SECTION OF ISA BUS
control bus

This diagram appears on page 239 of your textbook.



The four most important control signals of the IBM PC, provided by the 8288 chip, are

IOR (**I/O read**)
IOW (**I/O write**)
MEMR (**memory read**)
MEMW (**memory write**)

ENDS ; NINE

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