AN FPGA BASED 1-BIT ALL DIGITAL TRANSMITTER EMPLOYING DELTA-SIGMA MODULATION WITH RF OUTPUT FOR SDR

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***Abstract*— Software defined radio (SDR) is a rapidly evolving technology that is receiving enormous recognition and generating widespread interest in the telecommunication industry. In this paper, we present the architecture of an all-digital transmitter with radio frequency output targeting FPGA devices due to their reconfigurability and programmability. The all-digital transmitter directly synthesizes RF signal in the digital domain using Low Pass Delta Sigma Modulation (LPDSM). This eliminates the need for most of the analog and RF components. The all digital transmitter consists of one Cascaded Integrator Comb (CIC) filter, one LPDSM modulator and Digital Upconverter (DUC). The binary output waveform from the RF-ΔΣ modulator is centered at 800MHz with bit rate of 1.6 Gbps. The proposed architecture has been simulated and proved to have a satisfactory performance. Finally, a VHDL code is written for the LPDSM to demonstrate its implementation and verifying the simulation results.**

***Index Terms*— All Digital RF Transmitter, CIC filter, CORDIC, low pass Delta Sigma Modulator, SDR.**

I. INTRODUCTION

Wireless communication industry has experienced tremendous growth since the Early 1990's. The future wireless market demands addition of new services which provide more functionality for the end users. This growth is due to the major progress in the field of radio frequency (RF) integrated circuit design and the design trends. The development of system on-chip (SoC) design has led to integration of analog RF, analog baseband and digital signal processors on the same chip. This has resulted in low power devices with multi-purpose functionality. [1]

The wireless communication manufacturers and service providers all over the world invest in the development of new technologies and techniques to support the wireless standards. The traditional end user equipment usually supports transmission and reception of signals for only one standard. However, a major requirement for users and base stations that utilize more than one standard is a single chip set with minimum external components that can support those multiple standards. This would enable a single wireless device with adapted functionality. On the other hand, this will also furnish an appropriate platform for the 4G and beyond [1]. SDR Architecture has been proposed as a solution to support multiple wireless standards in a single chip [2]. The main goal of software radio transceiver is to perform the analog to digital (ADC) and digital to analog (DAC) conversion as close to the antenna as possible, with reconfigurable software programs running in the backend digital signal processor (DSP).

In the transmitter side, conventional linear power amplifiers (PA's) are generally power inefficient. This causes increased current drain in wireless hand-held equipment, reducing talk and standby time. Switched-mode PA's are more efficient, but they are nonlinear. This limits their usage with moderate or **high** peak-to-average ratio signals. The switching waveform (1-bit signal) is composed of the desired modulation plus out-of-band noise or harmonics, which can be filtered away. This enables the design of the transmitter using digital modules [3].

II. DIRECT DIGITAL RF TRANSMITTERS

Conventionally, the signal processing in wireless communication takes place in the base band digital domain. In order to transmit this signal, an upconversion is required. Upconversion can be accomplished in different techniques including analog mixing, combined digital/analog upconversion and direct digital conversion. The most promising technique for SDR is the direct digital conversion. This enables the implementation of the whole transmitter chain on a single reconfigurable device that supports multimode operation.

A. Direct digital conversion

In direct digital conversion shown in Fig. 1, the base band signal is generated using a digital modulator. Then it is upconverted with a digital upmixer to the required radio frequency. The D/A conversion is performed at RF and is followed by a linear power amplifier.

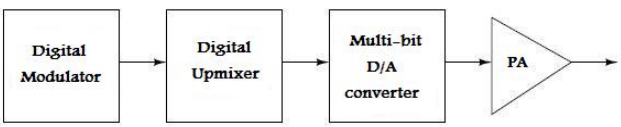

Fig. 1. Direct Digital Conversion Architecture

However, multi-bit D/A converter is susceptible to glitches and spurious noise (as the output frequency increases), which is difficult to remove by filtering [4]. Moreover parts of the digital circuits deal with RF frequencies, which require very high sampling frequency and causes high power dissipation.

B. Delta-sigma direct digital conversion

The transmitter architecture based on ΔΣ (Delta Sigma) Direct Digital Conversion shown in Fig. 2 is similar to the aforementioned Direct Digital Conversion, but the multi-bit D/A converter is replaced with a 1-bit ΔΣ D/A converter. ΔΣ Modulators are suitable only for relatively narrowband signals due to their noise shaping property. The signal bands under consideration are relatively narrow compared to the RF carrier frequency and therefore the narrowband nature of the ΔΣ D/A converter does not limit its usage. The 1-bit ΔΣ D/A converter is an all-digital circuit, which has several advantages over analog signal processing, such as flexibility, noise immunity, reliability, upgradeability and lower power consumption. In addition, the design, synthesis, layout and testing of digital systems can be highly automated [5]. The combination of a Direct Digital Frequency Synthesizer (DDFS) with a 1-bit ΔΣ-D/A converter is attractive in digital transmitters, because it allows the use of a switching-mode power amplifier, which attains higher efficiencies than linear ones [6].

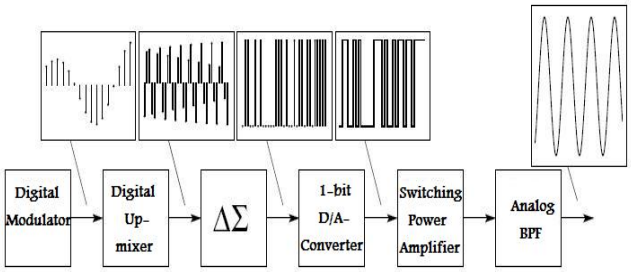

Fig. 2. Digital upconversion chain using ΔΣ DAC

III. PROPOSED ALL DIGITAL RF-ΔΣ TRANSMITTER

Many researches have published in the area of digital RF signal generation. However, only simulation results or non real-time test results have been presented in literature [3], [7], and [8]. In these works, the digital RF signals were computed offline and stored in pattern generator for the purpose of measurement. In this paper, we present the architecture and simulation of a real-time system that demonstrates the feasibility of implementing digital generation of RF signals. The use of Band-Pass Delta Sigma (BPDS) modulation to generate binary signals in the RF range is presented in [3]. As mentioned before binary coding can be used together with switched mode power amplifier to achieve higher efficiency compared with other types of PA technologies. The drawback of the architecture shown in Fig. 2 is that the BPDS modulator needs to be running at 4 times the output center frequency ($f_s = 4 \times f_c$). This high frequency which lies in the multigigahertz range can not be achieved by current FPGA devices. To accomplish such high frequency of operation, customized integrated circuits have to be carefully designed instead [9].

In the presented work, the target is the implementation of a complete system on an FPGA. BPDS is not suitable because of the high speed clock (in the gigahertz range) requirement. So we propose a different architecture that suits our target device. The proposed all-digital transmitter architecture is shown in Fig. 3. It consists of three major consecutive functional blocks: Cascaded Integrator Comb (CIC) interpolating filter, digital Low Pass Delta Sigma Modulator (LPDSM) and Digital Upconverter. CIC filter is a class of multirate filters used to achieve high interpolation (and decimation) rates and is efficiently implemented without multipliers [10]. In this work, it is used to filter the baseband signal and convert it to higher sampling rate suitable for the delta-sigma modulation process. This ΔΣ signal is then used to modulate a Direct Digitally Synthesized (DDS) carrier frequency. CIC is usually preceded by an FIR compensation filter that compensates the Sinc response of the CIC filter and achieves a flat frequency response with minimum distortion. LPDSM is used as a digital-to-digital converter, which converts a high precision representation of oversampled digital data to a low precision (1-bit) representation of the same data. This is the concept used in this work to build a single bit all digital transmitter that takes advantage of the high efficiency switching mode PAs. The digital upconverter consists of a Direct Digital Frequency Synthesizer (DDFS) based on Numerically Controlled Oscillator (NCO) and multiplier. Indeed the complete transmitter should still have a 1-bit DAC, power amplifier (switching mode) and a transmitting antenna. The interest in this paper is the design of the digital processing chain preceding the last three mentioned blocks.

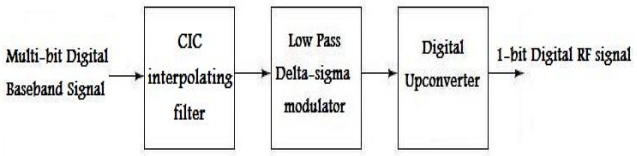

Fig. 3. Proposed all-digital RF−ΔΣ transmitter

The use of LPDSM before upconverting the signal (in the baseband) as shown in Fig. 3 makes the required clock of the modulator equals to the sampling rate of the oversampled digital input which will be in the megahertz range (depends on the input signal bandwidth and the required oversampling ratio (OSR)). In this case the implementation of the modulator on an FPGA will be viable. The all-digital transmitter presented in this paper directly synthesizes RF signal in the digital domain, the binary output waveform from digital upconverter is centered at 800MHz. The problem in implementing the digital upconverter still exists due to the requirement of a high speed internal clock which can not be achieved using FPGA devices. The relation between the output frequency of the NCO and its internal clock is:

$$F_{out} = \frac{S}{2^n} F_{clk} \qquad (1)$$

$$Where:\ F_{clk}\ is\ the\ NCO\ internal\ clock$$
$$F_{output}\ is\ the\ ouput\ frequency\ from\ the\ NCO$$
$$S\ \ is\ the\ phase\ increment\ value$$
$$n\ \ the\ size\ of\ the\ NCO\ internal\ register$$

According to Nyquist's sampling theorem, the maximum output frequency of the DDS cannot exceed 50% of the system clock. The NCO is designed to generate a digital sinusoidal waveform. As the needed output RF signal is binary (two levels), so the sinusoidal waveform should be quantized in only two levels (one sample from the positive half cycle and one sample from the negative half cycle). This means that the generated waveform is indeed a square wave. As a result the NCO operates on its maximum limit (the output frequency = half of the clock frequency). Since the carrier frequency is 800MHz as mentioned before, therefore the clock frequency required is 1.6GHz. This clock frequency is the operating clock of the proposed transmitter architecture, but it doesn't suit FPGAs (nowadays, maximum FPGA clock frequency does not exceed 800MHz while the required clock is 1.6 GHz).

The solution of this problem is that the output of the digital mixer is pre-computed and stored in a ROM. The ROM is addressed by the output sample from the ΔΣ modulator. In fact as will be seen in the simulation results, the output from the ΔΣ modulator is a binary (two level) signal. The output after mixing with the NCO waveform has two states, the same waveform either with phase 0˚ or with phase 180˚. So the patterns stored in the ROM are the NCO waveform itself and its inverted version. The parallel output from the ROM is then applied to a high speed parallel to serial converter to obtain the output bit stream. In this case the actual processing of the FPGA is the output sampling frequency from the ΔΣ modulator which is in the megahertz range. Thus, the feasibility of the system implementation on FPGA can be easily achieved.

IV. System Model & Simulation Results

The entire all digital transmitter shown in Fig. 3 was designed and tested using the Matlab signal processing blockset. In our simulation environment, we apply a discrete single tone sinusoidal signal as an input. The target of simulation is to test the functionality of the system and to select the maximum input signal frequency that gives a satisfactory performance with respect to efficient processing of the FPGA. The system performance is measured by the SQNR (signal-to-quantization noise ratio) of the ΔΣ modulator whereas the efficient operation of FPGA is defined in terms of using it with the maximum permissible clock rate. The Simulink Discrete Time (DT) model implementation of the ΔΣ modulator is shown in Fig. 4. The modulator is third order with all zeros of the noise transfer function at DC (low pass). The used architecture of the loop filter is a cascade of resonators with distributed feedback (CRFB) [11]. The coefficients of the modulator are obtained using a Matlab design toolbox.

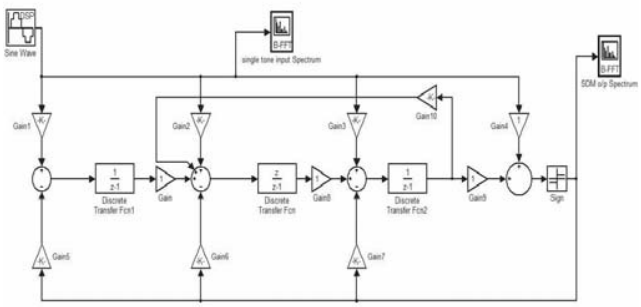

Fig. 4. A DT model for a 3rd order CRFB LPDSM

The modulator is simulated with different OSRs to monitor the effect on the SQNR. When the OSR of the signal increases, the quantization noise is spreaded over a wider bandwidth, so the quantization noise power will be reduced in the band of interest, thus the SQNR is increased. This concept is verified in Fig. 5. The SQNR is calculated using the describing function method of Ardalan and Paulos [12].

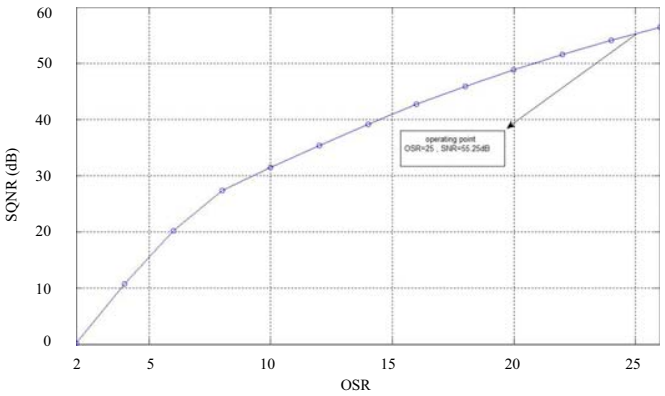

Fig. 5. OSR versus SQNR of the modulator

On the other hand, as a result of practical design issues, FPGA does not utilize its maximum operating clock. The practical value mostly used is around 100MHz. So our design is restricted to this frequency as the sampling frequency of the signal. Taking this factor into consideration, the maximum signal frequency (Fm) that gives a satisfactory SQNR of 55.25dB is 2MHz. This is equivalent to OSR of 25.

The input and output spectrum of the ΔΣ modulator without the CIC compensation is shown in Fig. 6. The effect of the high ripples (Sinc response) in the stop band of the CIC filter is shown in the spectrum of the oversampled single tone input. This produces a high frequency harmonics. The observed output spectrum from the modulator is identical to the input in the band of interest. The noise due to 1-bit quantization is shaped out of the band of interest at higher frequencies. This high frequency noise can be easily rejected using a digital low pass filter. The input/output spectrum after adding the compensator is shown in Fig. 7. The high frequency components resulted from the CIC filter is totally attenuated by the high stop band attenuation of the compensator.

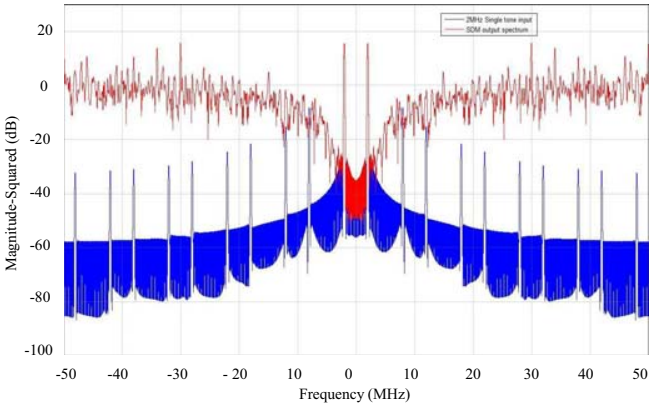

Fig. 6. Input/output spectrum of the modulator without CIC compensator

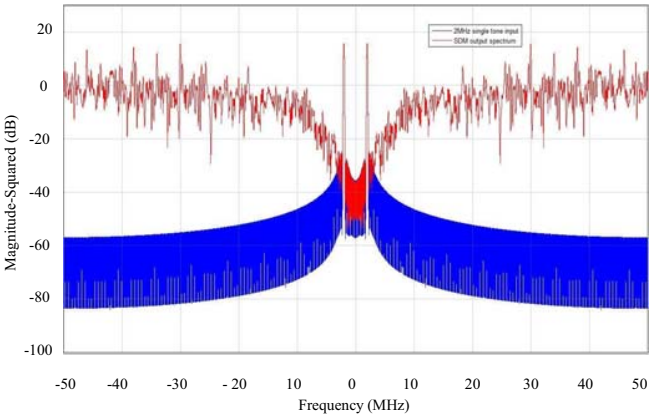

Fig. 7. Input/output spectrum of the modulator with CIC compensator

These effects can be seen also in the time domain plots in Fig. 8 and Fig. 9. In these Figures, the modulator function is obvious as the high resolution sinusoidal waveform is converted into a 1-bit binary waveform. This explains the appearance of the high frequency quantization noise in the spectrum (outside the band of interest).

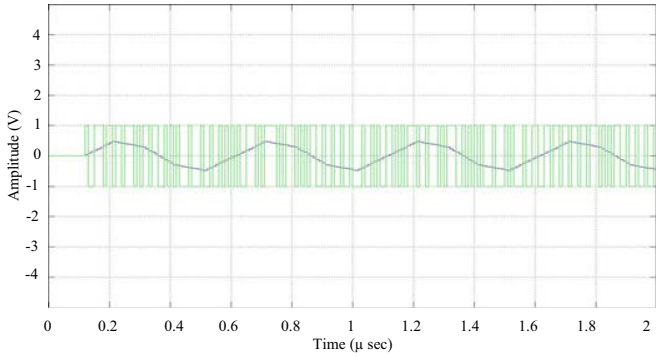

Fig. 8. Input/output waveforms of the modulator without CIC compensator

As can be inferred from the figures, the effect of CIC compensator is smoothing of the time domain signal due to suppression of the high frequency components. Moreover, the additional delay of the compensating filter can be noticed in Fig. 9.

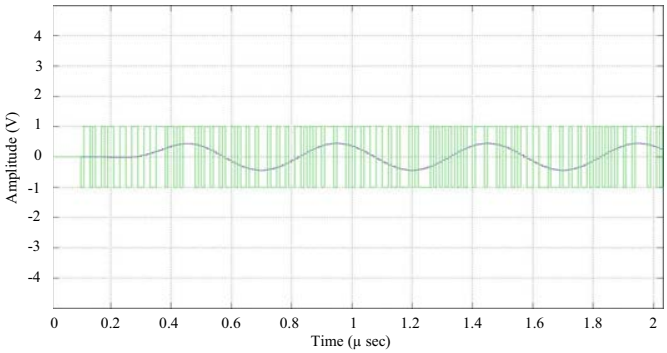

Fig. 9. Input/output waveforms of the modulator with CIC compensator

The complete model of the proposed all-digital transmitter is shown in Fig. 10. The NCO block is designed to generate a digital carrier frequency of 800MHz which is multiplied by the output from the modulator to shift the base band spectrum by the carrier frequency.

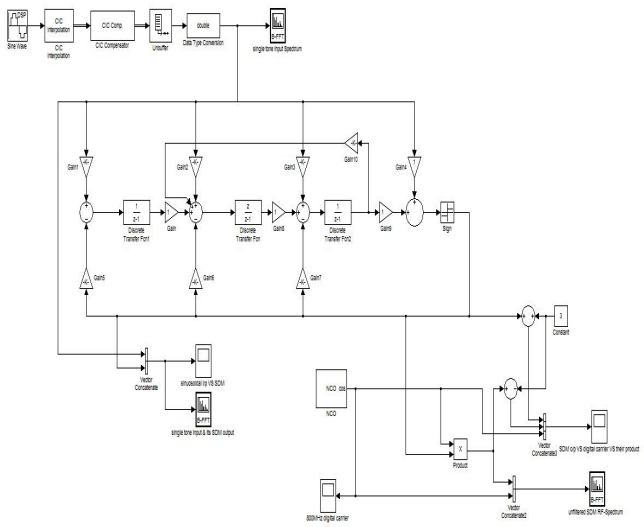

Fig. 10. The DT model of all-digital RF−ΔΣ transmitter

The spectrum of the carrier signal with the RF output signal (after the mixing operation) is illustrated in Fig. 11. This spectrum illustrates the definition of the modulation process, as being just a frequency shift of the baseband spectrum shown in Fig. 7 by the carrier frequency. Both of the single tone spectrum and the shaped quantization noise are centered at 800MHz. The use of NCO gives the ability to digitally reconfigure the transmitter to the intended band of operation. This is achieved by changing the phase increment value (S) in equation 1. The mixing operation between the modulator output and the digital carrier in time domain is illustrated in Fig. 12. The upper waveform represents the modulator output while the middle is the NCO output. The last waveform is the mixing result. It is a simple multiplication and results in a binary form.

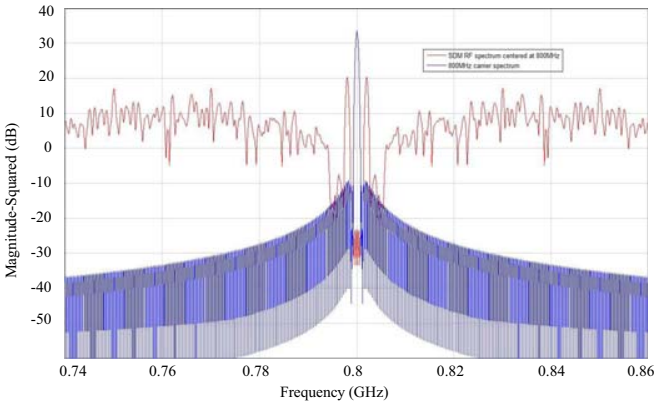

Fig. 11. RF spectrum centered at 800MHz

So the final RF signal is obtained in a binary format and thus can be represented with a single bit. The DC shift appeared in the figure is done intentionally to view the signals in a clear view but practically the DC offset is zero for the three signals.

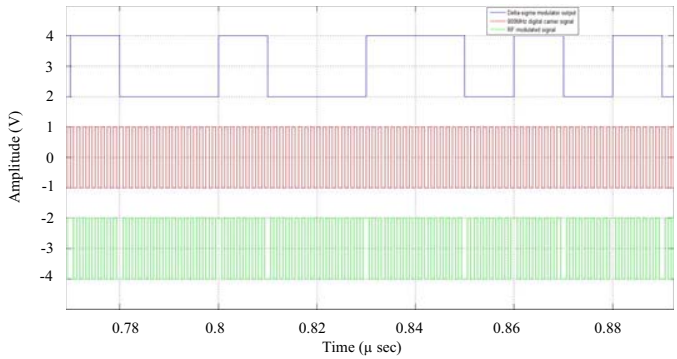

Fig. 12. Mixing operation waveforms

V. Modulator Implementation

In this section, the modulator model presented in Fig. 4 is designed using structural architecture VHDL code. The used tool was FPGAdv Pro 5.2 provided by Mentor Graphics. This was for the purpose of verifying the functionality of the FPGA processing compared to the Matlab operation. In addition, a VHDL code is also written for a DDFS based CORDIC (Co-Ordinate Rotation Digital Computer) algorithm [13] to drive the modulator with a sinusoidal input as described in section IV. The top level design of the modulator connected to the DDFS is shown in Fig. 13. Concerning the coefficients of the modulator, a scaling factor is introduced to the coefficients with the same value used to represent the sample points generated from the DDFS. Fig. 14 shows the simulation result of the modulator with the DDFS architecture presented in Fig. 13 in an analog view. This simulation is done using the Modelsim simulator. The input phase angle to the CORDIC block is represented in 18-bits, whereas the sinusoidal calculation (CORDIC output) is represented in 32-bits. The input clock running the modulator and the DDFS is 125MHz. The frequency of the CORDIC output (sinusoidal waveform) is 1.953125MHz. Thus the OSR of the sinusoidal waveform is 32. This ratio is intentionally taken to obtain an integer value of the phase increment (S) found in equation 1.

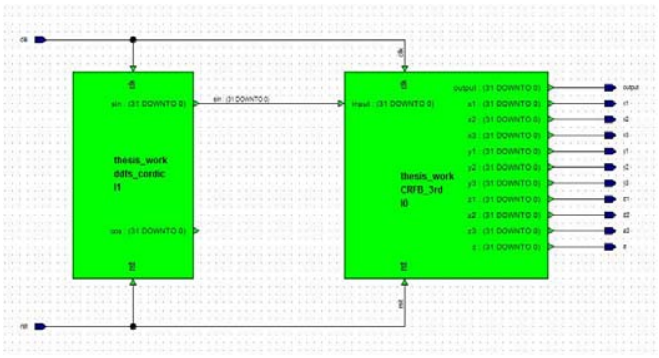

Fig. 13. Top level Architecture of the Modulator drived with CORDIC based DDFS

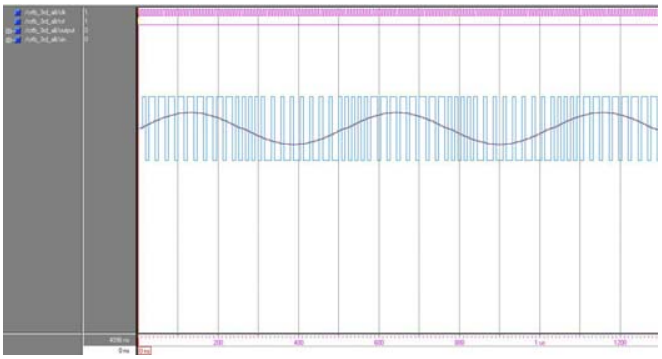

Fig. 14. Functional Simulation of the Modulator drived with CORDIC based DDFS

VI. Conclusion

In this paper the problem of designing all digital transmitter for SDR applications is dealt with. We propose a new method of synthesizing the RF signals directly in the digital domain using low pass ΔΣ conversion. The transmitter is capable of encoding multi-bit baseband signals into single bit RF signals. This enables the use of switching mode power amplifiers which possess higher efficiencies than conventional linear amplifiers mostly used in transmitters. The low processing rate of the ΔΣ modulator eases the implementation of the whole transmitter on an FPGA. The resulting output binary data has a rate of 1.6 Gbps and centered at 800MHz. This output frequency will enable the all-digital transmitter to realize an optimum SDR communication system in the future. In the outgoing research, the designed transmitter will be completely implemented and tested on an FPGA.

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