FPGA Prototyping of Digital RF Transmitter Employing Delta Sigma Modulation for SDR

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Abstract

The term software defined radio (SDR) is usually used to refer to a radio transceiver in which its key parameters are defined in software and having its fundamental aspects reconfigurable by upgrading that software. SDR architecture has been proposed as a solution to support multiple wireless standards on a single platform. In this paper, we present the architecture of an all-digital transmitter with radio frequency (RF) output targeting FPGA devices due to their reconfigurability and reprogrammability. The all-digital transmitter directly synthesizes RF signal in the digital domain using Low Pass Delta Sigma Modulation (LPDSM). This eliminates the need for most of the analog and RF components. The all digital transmitter consists of one Cascaded Integrator Comb (CIC) filter, one LPDSM modulator and Digital Upconverter (DUC). The binary output waveform from the RF-ΔΣ modulator is centered at 800MHz with bit rate of 1.6 Gbps. The proposed architecture has been simulated to prove the idea and test its performance. Finally, the proposed architecture is designed using VHDL design entry and ready for download on the target FPGA.

Index Terms— All Digital Transmitter, CIC filter, CORDIC, low pass Delta Sigma Modulator, SDR, DDFS, NCO, MGT

1. INTRODUCTION

SDR is a rapidly evolving technology that is receiving enormous recognition and generating widespread interest in the telecommunication industry. Over the last few years, analog radio systems were replaced by digital radio systems for various radio applications in military, civilian and commercial spaces. In addition to this, programmable hardware modules are increasingly being used in digital radio systems at different functional levels. SDR technology aims to take advantage of these programmable hardware modules to build open-architecture based radio system software.

Traditional hardware based radio devices [1] limit cross-functionality and can only be modified through physical intervention. This results in higher production costs and minimal flexibility in supporting multiple waveform standards. In contrast, SDR technology provides an efficient and comparatively inexpensive solution to this problem, allowing multi-mode, multi-band and/or multi-functional wireless devices that can be enhanced using software upgrades.

The most common attribute used to define SDR is a radio transceiver that can perform the analog to digital (ADC) and digital to analog (DAC) conversion as close to the antenna as possible, with reconfigurable software programs running in the backend digital signal processor (DSP) [2]. In the transmitter side, conventional linear power amplifiers (PA's) are generally power inefficient. This causes increased current drain in wireless hand-held equipment, reducing talk and standby time. Switched-mode PA's are more efficient, but they are nonlinear. This limits their usage with moderate or **high** peak-to-average ratio signals. The switching waveform (1-bit signal) is composed of the desired modulation plus out-of-band noise or harmonics, which can be filtered away. This enables the design of the transmitter using digital modules [3].

2. ALL DIGITAL TRANSMITTER ARCHITECTURE

Conventionally, the signal processing in wireless communication takes place in the base band digital domain. In order to transmit this signal, an upconversion is required. Upconversion can be

accomplished in different techniques including analog mixing, combined digital/analog upconversion and direct digital conversion. The most promising technique for SDR is the direct digital conversion. This enables the implementation of the whole transmitter chain on a single reconfigurable device that supports multimode/multiband operation.

2.1 Direct digital upconversion architecture

Conventional upconversion techniques used to modulate information signals in the analog domain by multiplication with analog carrier. This is usually implemented using customized ASIC circuits that can't be reconfigured for different functionalities. In the direct digital conversion shown in Fig. 1, the base band signal is generated using a digital modulator. Then it is upconverted with a digital upmixer to the required radio frequency. The D/A conversion is performed at RF and is followed by a linear power amplifier that outputs the final high power RF signal. This all digital architecture can support different modes of operation in terms of the modulation scheme, transmitting frequency, signal processing algorithms and communication protocols through simple programming of the digital parts. However, a major drawback of this architecture is that the multi-bit D/A converter is susceptible to glitches and spurious noise in this high conversion frequency (RF frequency), which is difficult to remove by filtering [4]. Also linear power amplifiers consume a lot of power which make it inefficient in portable handheld (power limited) devices.

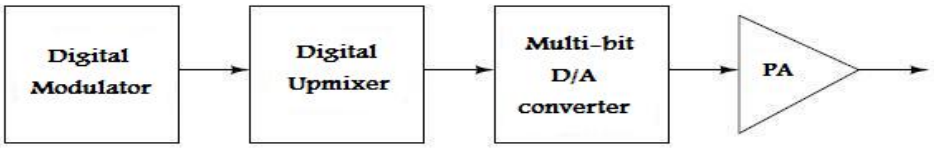

Fig. 1. Direct Digital Upconversion Architecture

2.2 Band Pass Delta-Sigma direct digital upconversion

A more suitable architecture found also in literature that solves the drawbacks of the previously discussed one, is the Band Pass Delta Sigma (BPDS) Conversion shown in Fig. 2. It is similar to the aforementioned Direct Digital Conversion, but the multi-bit D/A converter is replaced with a 1-bit ΔΣ D/A converter. The combination of a Direct Digital Frequency Synthesizer (DDFS) with a 1-bit ΔΣ-D/A converter is attractive in digital transmitters, because it allows the use of a switching-mode power amplifier, which attains higher efficiencies than linear ones [5].

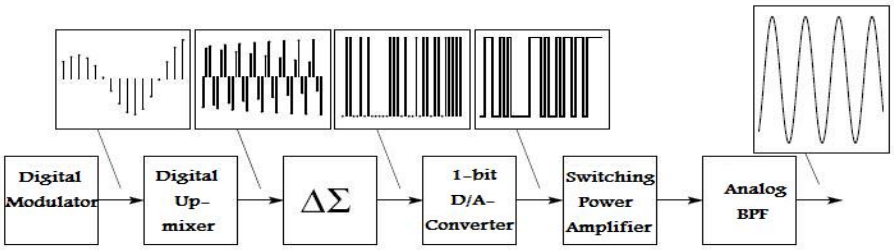

Fig. 2. BPDS based all digital upconversion architecture

Many researches have published works in the area of digital RF signal generation. However, only simulation results or non real-time test results have been presented in literature [3], [6], and [7]. In these works, the digital RF signals were computed offline and stored in pattern generator for the purpose of measurement. The use of BPDS modulation to generate binary signals in the RF range has been first presented in [3]. The drawback of this architecture is that the BPDS modulator needs to be running at 4 times the output center frequency ($f_s = 4 \times f_c$). This high frequency typically lies in the giga-hertz range. Thus the implementation of transmitter becomes a very difficult task (nearly impossible) using current FPGA devices (or any programmable device). To accomplish such high frequency of operation, customized integrated circuits have to be carefully designed instead [8]. Another architecture based on Pulse Width Modulation (PWM) used to generate binary RF signals was first presented in [9] and then implemented on an FPGA in [8]. In contrast with BPDS modulation, this

architecture is suitable for implementation on programmable devices as it requires much lower clock frequency.

3. PROPOSED ALL DIGITAL TRANSMITTER EMPLOYING LOW PASS Δ-Σ MODULATION

In this work, we present the architecture, simulation and implementation of a novel all digital transmitter architecture with RF output employing delta sigma modulation. The target is the implementation of the proposed architecture on an FPGA. As mentioned before, BPDS modulation is not suitable for this task because of the high speed clock requirement. So we propose a different architecture that suits our target device. The proposed all-digital transmitter architecture is shown in Fig. 3. It consists of three major consecutive functional blocks: Cascaded Integrator Comb (CIC) interpolating filter, digital Low Pass Delta Sigma Modulator (LPDSM) and Digital Upconverter.

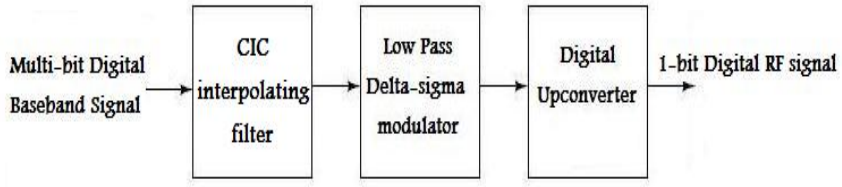

Fig. 3. Proposed all-digital RF transmitter based on LPDSM

The CIC filter [10] is used to filter the baseband signal and convert it to higher sampling rate suitable for the delta-sigma modulation process. The oversampling ratio (OSR) of the CIC filter will determine the spectral purity of the LPDSM output signal. This is the main factor affecting the quality of the delta sigma conversion process [11]. The LPDSM is used as a digital-to-digital converter, which converts a high precision representation of oversampled digital data to a low precision (1-bit) representation of the same data with the quality being preserved. This is the concept used in this work to build a single bit all digital transmitter that takes advantage of the high efficiency switching mode PAs. The digital upconverter consists of a Direct Digital Frequency Synthesizer (DDFS) based on Numerically Controlled Oscillator (NCO) and multiplier.

The major difference between this architecture and its BPDS counterpart is using the delta sigma modulator before upconverting the signal (in the baseband). This makes the required clock of the modulator equals to the sampling rate of the oversampled digital input which will be in the megahertz range (depends on the input signal bandwidth and the required oversampling ratio (OSR)). In this case the implementation of the modulator on an FPGA will be an easy task. The all-digital transmitter presented in this paper directly synthesizes the RF signal in the digital domain; the binary output waveform obtained from the digital upconverter is centered at 800MHz.

4. SYSTEM MODEL & SIMULATION RESULTS

For the purpose of verifying the idea, the proposed transmitter architecture presented in Fig. 3 was designed and tested using the Matlab signal processing blockset. In our simulation environment, we apply a discrete single tone sinusoidal signal as an input. The target from the simulation is to test the functionality of the system and to select the maximum input signal frequency that gives a satisfactory performance with respect to efficient processing of the FPGA. The system performance is measured by the SQNR (signal-to-quantization noise ratio) of the ΔΣ modulator (which depends on the OSR of the input signal) whereas the efficient operation of FPGA is defined in terms of using it with the maximum permissible clock rate. The Simulink Discrete Time (DT) model of the ΔΣ modulator is shown in Fig. 4. The modulator is third order with all zeros of the noise transfer function at DC (hence, named low pass). The used architecture of the loop filter is a cascade of resonators with distributed feedback coefficients (CRFB) [11]. The coefficients of the modulator are obtained using a Matlab design toolbox. The modulator is simulated with different OSRs to monitor the effect on the SQNR. The SQNR is calculated using the describing function method of Ardalan and Paulos [12]. According to experimental trials, our available FPGAs clock rate didn't exceed 100 MHz. So our design is restricted to this frequency as the sampling frequency of the signal. Taking this factor into

consideration, the maximum signal frequency (Fm) that gives a satisfactory SQNR of 55.25dB is 2MHz. This is equivalent to OSR of 25 and effective number of bits (ENOB) of 9 [11].

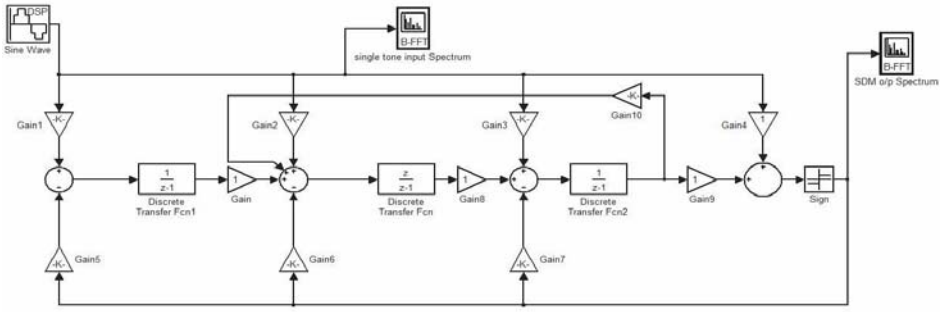

Fig. 4. A DT model for a 3rd order CRFB LPDSM

After applying this 2MHz sinusoid to the CIC filter (giving an OSR of 25) and the LPDSM (in Fig. 4), the input/output spectrum obtained is as shown on Fig. 5. The observed output spectrum from the modulator is identical to the input in the band of interest. The noise due to 1-bit quantization is shaped out of the band of interest at higher frequencies (this is known by the modulator noise shaping property). This effect can be seen also in the time domain as illustrated in Fig. 6. As we can observe, the modulator function is obvious, converting the high resolution sinusoidal waveform is into a coarse quantized binary waveform. This explains the appearance of the high frequency quantization noise in the spectrum (outside the band of interest) of Fig. 5.

The complete model of the proposed all-digital transmitter is shown in Fig. 7. The NCO block is designed to generate a digital carrier frequency of 800MHz which is multiplied by the output from the modulator to shift the base band spectrum by the carrier frequency. In order to obtain the final RF signal in a binary from, we operate the NCO on its maximum limit, which means that the synthesized output signal frequency is half of its operating clock frequency [13]. This means that the synthesized waveform is indeed a square wave. Since the carrier frequency is 800MHz as mentioned before, therefore the clock frequency required is 1.6GHz. This gives an output data rate of 1.6 Gbps.

The spectrum of the carrier signal with the RF output signal (after the mixing operation) is illustrated in Fig. 8. It is a frequency shift of the baseband spectrum (in Fig. 5) by the carrier frequency. The mixing operation between the modulator output and the digital carrier in time domain is illustrated in Fig. 9. The upper waveform represents the modulator output while the middle is the NCO output. The last waveform is the mixing result. It is a simple multiplication and results in a binary waveform. So the final RF signal is obtained in a binary format and thus can be represented with a single bit. Consequently we took the advantage of this simple upconversion process in the hardware architecture by replacing the high speed DUC with a simple mapping ROM that stores the multiplication result instead of performing it [13]. This reduces the processing clock of the design to the sampling frequency of the signal.

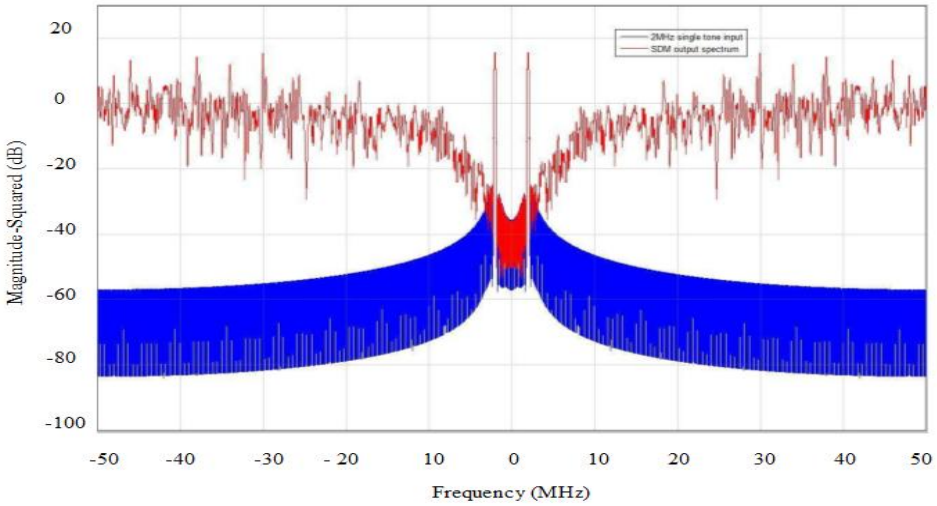

Fig. 5. Input/output spectrum of the LPDSM with CIC interpolation

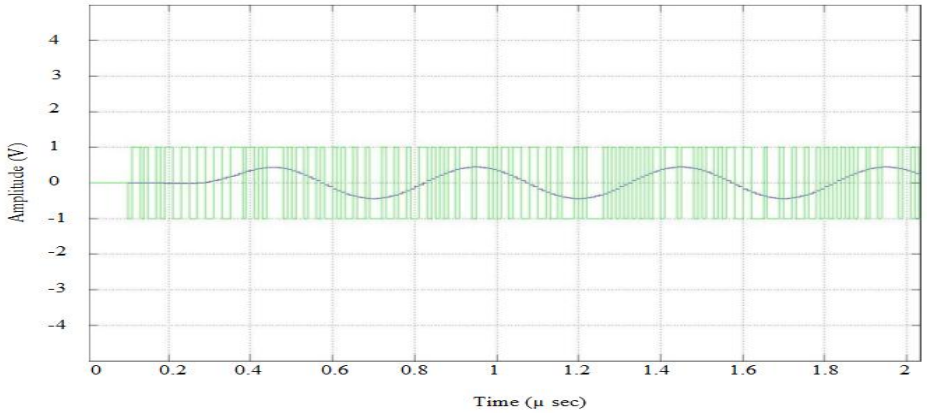

Fig. 6. Input/output waveforms of the LPDSM with CIC interpolation

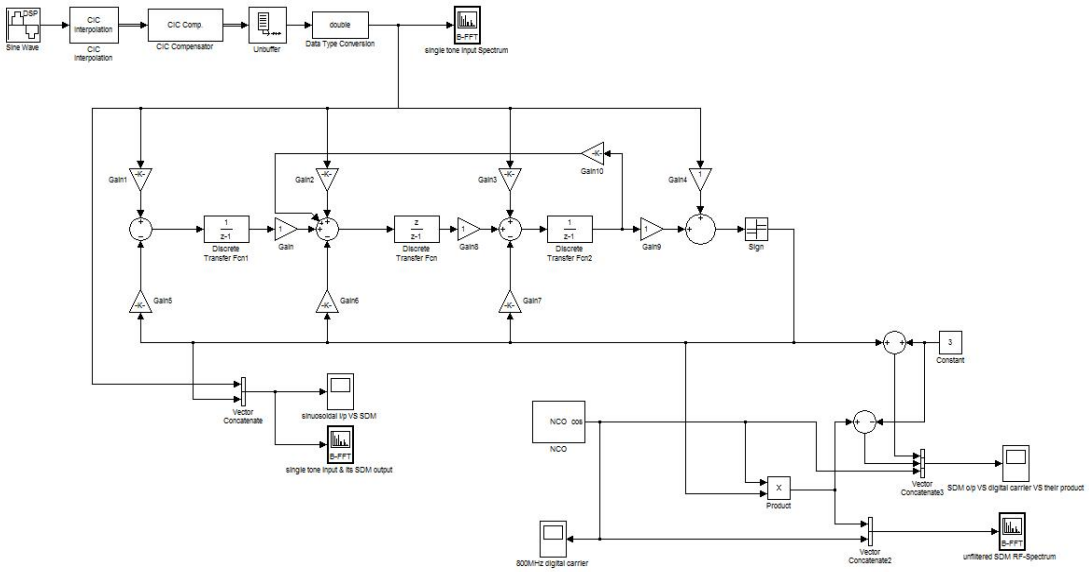

Fig. 7. The DT model of the proposed all digital transmitter

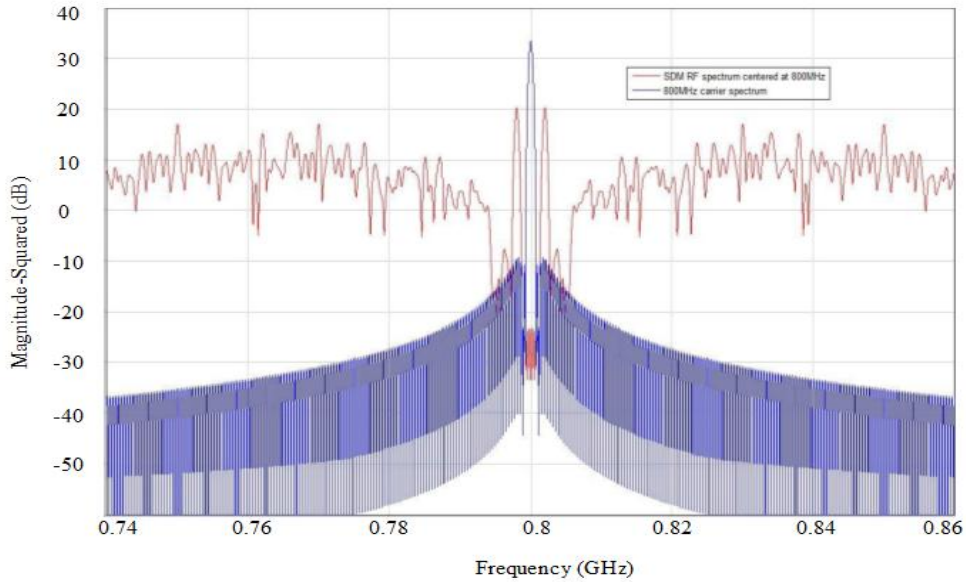

Fig. 8. RF spectrum centered at 800MHz

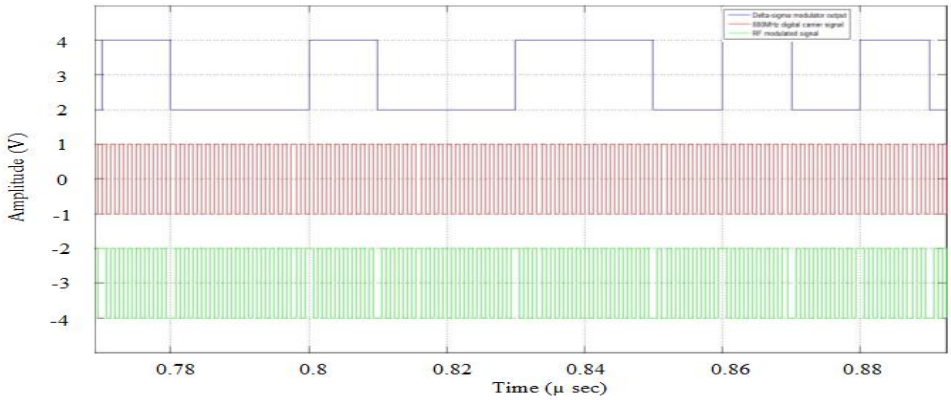

Fig. 9. Upconversion process in the time domain

5. TRANSMITTER IMPLEMENTATION

In this section the proposed transmitter model is converted to a hardware architecture that can be mapped on our target FPGA device. This architecture is illustrated in Fig. 10. We use a ROM based DDFS to provide the transmitter with the 2MHz sinusoidal input. The output is represented using 32-bits. For simplicity we use the DDFS to oversample the signal instead of using a CIC stage [13]. The 32-bits are then applied to the LPDSM which converts it to 1-bit instead. This bit is then used to address the RF-ROM with 8-bit size for either zero phase sequence or 180^o phase sequence representing the upconversion process [13]. This is equivalent to mixing with 400 MHz carrier frequency and 800Mbps serial output. Increasing the ROM size gives higher mixing frequency and data rate as well. The ROM parallel output is then converted to the final bit stream using a parallel-to-serial (p/s) converter incorporating 3-bit counter and 8x1 multiplexer. This makes the effective clock frequency of the design be equal to the sampling frequency of the signal (100 MHz). Concerning the high speed clock of the p/s converter, many families form Xilinx recently provide this high switching speed using on chip Multi-Gigabit-Transceiver (MGT) [8].

The presented architecture in Fig. 10 is then described using VHDL design entry. The used tool was FPGAdv Pro 5.2 provided by Mentor Graphics. This was for the purpose of verifying the functionality of the FPGA processing compared to the Matlab operation. The obtained architecture is shown in Fig. 11. After running this design using the Modelsim simulator, the obtained results were as shown in Fig. 12 and Fig. 13. Fig. 12 shows the analog view of the synthesized sinusoidal signal form the ROM based DDFS and its equivalent output from the LPDSM just as obtained from the Matlab Simulation. The synthesized sinusoidal signal is of frequency 1.5625MHz (640nsec), taking into account that the phase accumulator size is chosen to be 10 bits. Fig. 13 shows a digital view for the outputs obtained from the DDFS, LPDSM, RF- ROM and the p/s converter. The output from the DDFS is obtained at the rising edge of the CLK, followed by the outputs from the LPDSM and the RF-ROM at the rising edges of the next two clocks

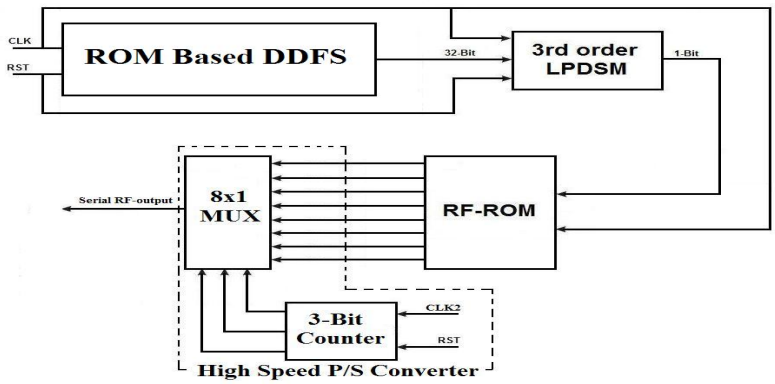

Fig. 10. Proposed FPGA all digital transmitter architecture with serial RF-output

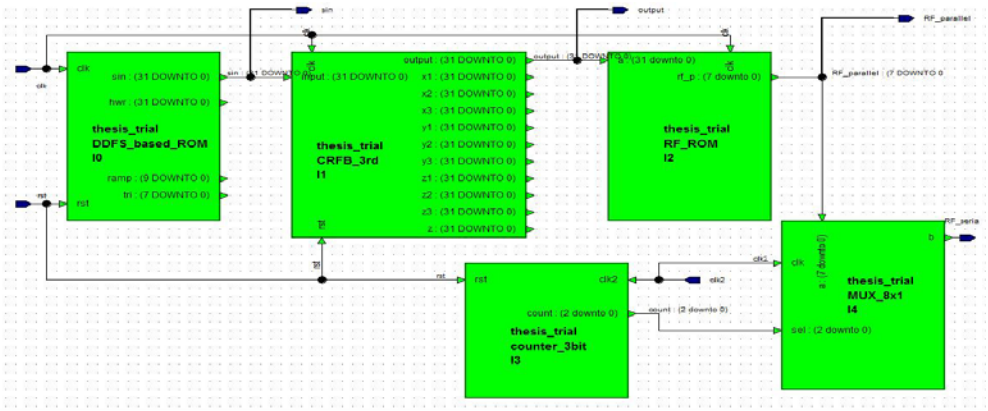

Fig. 11. VHDL architecture of the all digital Tx with serial RF output utilizing ROM based DDFS

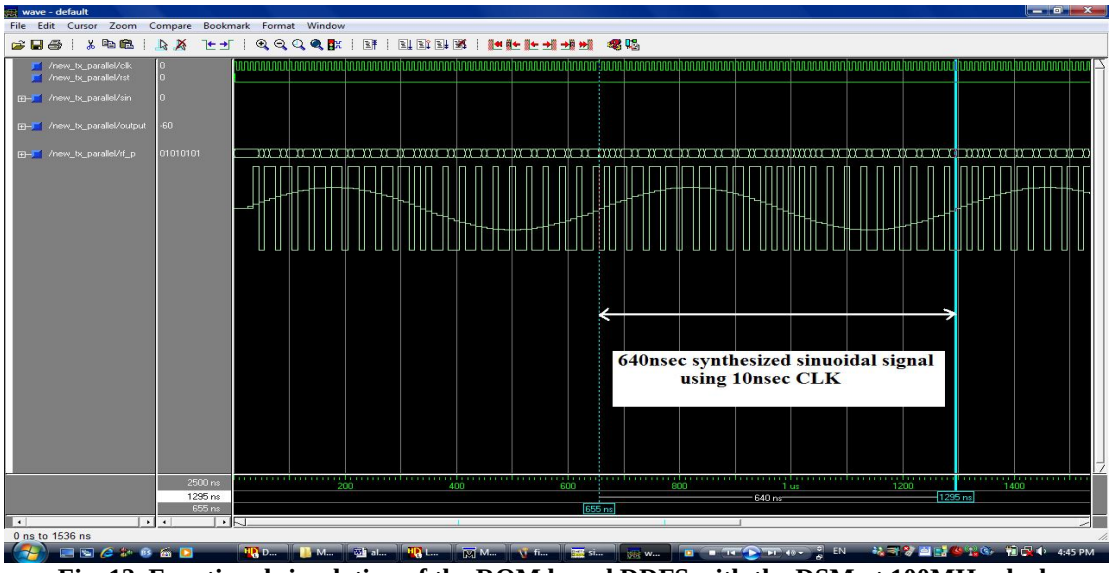

Fig. 12. Functional simulation of the ROM based DDFS with the DSM at 100MHz clock

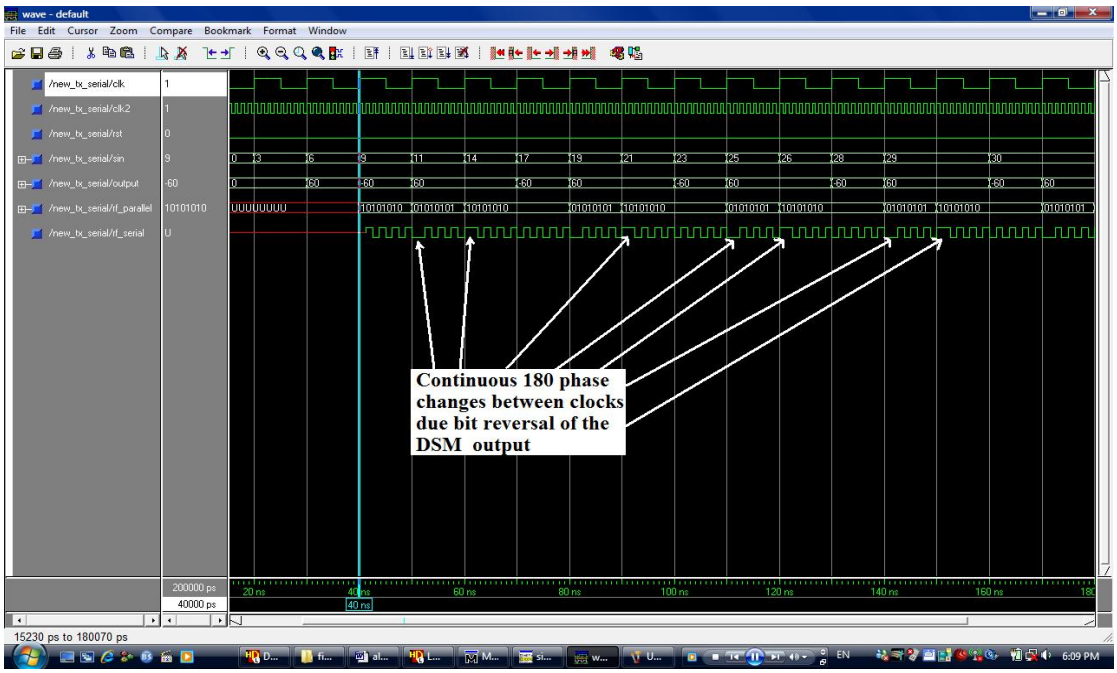

Fig. 13. Functional simulation of the all digital Tx with serial RF output running at 100MHz effective clock and a data rate of 800Mbps

CONCLUSION

In this paper, we present the architecture of an all-digital transmitter with radio frequency output targeting FPGA devices due to their suitability for SDR applications. We propose a novel technique of synthesizing the RF signals directly in the digital domain using low pass $\Delta\Sigma$ conversion instead of the impractical BPDS counterpart. The transmitter is capable of encoding multi-bit baseband signals into single bit RF signals. This enables the use of switching mode power amplifiers which possess higher efficiencies than conventional linear amplifiers mostly used in transmitters. The resulting output binary data from the simulation has a rate of 1.6 Gbps and centered at 800MHz. The hardware architecture parameters are chosen to obtain a data rate of 800Mbps centered at 400MHz. The architecture is highly flexible in terms of the data rate and RF carrier frequency which makes it a good starting point for realizing a multiband SDR communication system in the future. In the outgoing research, the designed transmitter will be completely implemented and tested on an FPGA to serve a real time communication protocols.

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