Design and Implementation of a Real-time Sleep Stage Monitoring System for Narcolepsy Diagnosis

Fadi S. Ayad[*], Hanady H. Issa[*], Mohamed S. El-Mahallawy[*], Khaled A. Shehata[*]

[*]*Department of Electronics and Communications Engineering*
[*]*Arab Academy for Sciences, Technology and Maritime Transport "AASTMT", Cairo Branch*
fadiayad@aast.edu, Hanady.issa@gmail.com, Mahallawy@aast.edu, K_shehata@aast.edu

Abstract – **A number of illnesses that affect people's daily life are caused by numerous sleep disorders which usually have common symptoms. In order for a physician to determine the correct diagnosis and its proper treatment, an overnight sleep analysis is usually performed. The scope of this paper is to design and implement a portable system that will assist Narcoleptic patients, in real-time, to aid them into leading a more productive life. The Feature Extraction Unit of the system is implemented on a Xilinx FPGA chip with a maximum error rate of 0.1618%. The classification method used is based on Support Vector Machine (SVM) algorithm, achieving an accuracy rate above 90%.**

Keywords: Biomedical, Sleep Disorders, Support Vector Machine, FPGA, Narcolepsy.

I. INTRODUCTION

According to the manual of sleep standards [1], in a normal sleep cycle the alertness level consists of two general stages; none-rapid eye movement (NREM) and rapid eye movement (REM). The NREM stage represents the transition from wakefulness to deep sleep going through 4 different stages of sleep alertness; while the REM stage is characterized as the stage in which dreaming occurs.

Narcolepsy is a chronic neurological disorder that affects the sleep cycle causing many symptoms such as uncontrollable episodes of daytime sleepiness (EDS), loss of muscle tone (Cataplexy), sleep paralysis, and hallucinations [2]. EDS being the dominant symptom is characterized by the interference of wakefulness and dreaming states.

However; since different sleep disorders may exhibit similar symptoms, detailed analysis of the electroencephalogram (EEG) spectrum is required to properly detect any unusual pattern. Classically this analysis is conducted as such: The process at which a patient spends the night at a sleep clinic connected to number of electrode sets; followed by a time consuming visual scoring of the recorded data by a physician.

Medical research clearly states that real-time monitoring of the EEG spectrum would improve the treatment of many sleep disorders such as Narcolepsy [2].

In [3] and [4] a study of the different classification method was introduced for the sleep stage classification. However, in [4], an implementation was introduced as a prototype using a single computer board with an Intel processor as its core.

This paper is dedicated to design and to implement a fully functional portable real-time system; aiming to help patients with such sleep disorders to overcome their difficulties and to improve their lifestyle and productivity. It includes the following sections: Section II in which the proposed system design is described in details, explaining the chosen algorithms. Section III discusses the hardware VHDL implementation of the proposed system. In Section IV the simulation of the system and its results are discussed, the system is tested on a number of pre-recorded and scored EEG data for healthy and narcoleptic patients. Finally Section V is dedicated to the conclusion and the discussion of the results.

II. PROPOSED DESIGN

Any system that processes analog signals consists of a digital to analog conversion unit, a digital signal processing unit, and finally an output interface unit with an optional memory for data logging. The scope of this paper focuses on the Data Processing Unit, which is composed of a Feature Extraction Unit and a Classifier Unit. Figure 1, illustrates the proposed block diagram for this system.
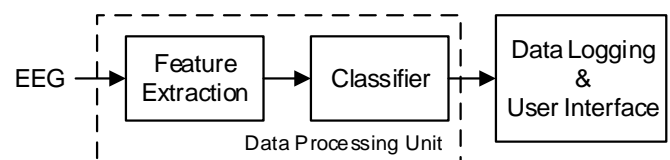

Figure 1: Functional Block Diagram of Proposed Design

For all intelligent systems there are two modes of operation, the training mode at which the system learns how to properly classify any given data to its corresponding output, and the testing mode of operation at which the system applies its learnt data to obtain an accurate classification.

As it is illustrated in figure 2, these two modes of operation are similar; however the learning process is an offline task that is done on a computer, it requires the input EEG stream along with its pre-scored values. Thus only the testing mode is implemented.
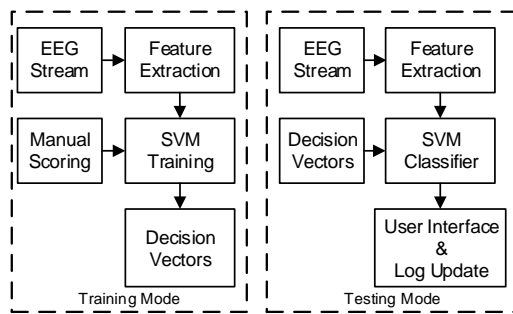
Figure 2: Modes of Operation Flow Chart

A. Data Preparation

In order to train and to test the system, a number of complete EEG recordings is acquired from PhysioBank medical database. These recordings – stored in the European Data Format (EDF) – are for a number of healthy and narcoleptic subjects. According to the manual of sleep standards [1], the EEG spectrum can be used to describe each state of alertness from awake to REM sleep. The differential signal C3-A2 according to the 10-20 electrode placement system, is the standard signal used in sleep monitoring [5]; therefore a single channel EEG is selected for this system. The recorded data collected from the database were sampled at 128 Hz.

B. Feature Extraction Unit

Feature selection is crucial to the classification process, since selection of wrong features, leads to classification error. Due to the localization of the features in both time and frequency, Fast Fourier Transform (FFT) is not suitable for processing of the EEG spectrum. Wavelet Transform (WT) is found to be the most suitable algorithm as it specifies the presence of each frequency as well as its time allocation [2] [3] [4] [6] [7] [8]. Table 1 summarizes the EEG sub-bands and their frequencies.

TABLE I. EEG FREQUENCY BANDS

EEG Sub-Bands	Start Frequency	End Frequency
Delta	00.39	03.13 Hz
Theta	03.13	08.46 Hz
Alpha	08.46	10.93 Hz
Spindle	10.93	15.63 Hz
Beta1	15.63	21.88 Hz
Beta2	21.88	37.50 Hz

The Feature Extraction Unit illustrated in figure 3, consists of two operations, extracting the Wavelet Packet Transform (WPT) coefficients, and calculating the desired features for each epoch. The RAM Unit is used to store the features while the Feature Extraction Unit starts working on the next epoch.
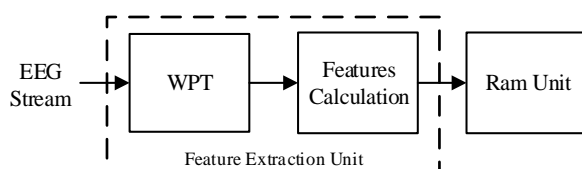

Figure 3: Feature Extraction Unit Proposed Block Diagram

1- Wavelet Packet Transform Unit provides a multi-resolution and time-frequency analysis for the EEG data. A full decomposition tree may be generated using the WPT by repeatedly applying a pair of high pass and a low pass filters followed by a decimation by 2 [9]. Filters applied must be orthogonal, in this design Debauchee second order filter are applied. Figure 4 illustrates the WPT tree followed in this design [2].
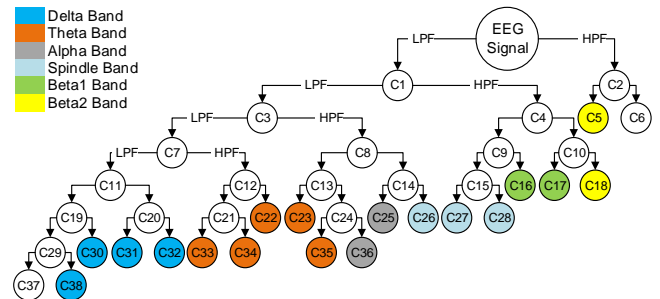

Figure 4: Proposed Wavelet Packet Tree

2- Once all the sub-band coefficients of a complete epoch are extracted, a total number of 22 features are calculated as follows [2]:

  1- The energy of each band.
  2- The total energy in all bands.
  3- Ratio of different energy values
  4- The mean of the absolute values of each band.
  5- The standard deviation for each band.

C. Classification Unit

According to [4] and [10], SVM algorithm proves to be a more effective classifier that achieves higher accuracy rates compared to other classification techniques. The SVM essentially maps the feature to a higher dimensional space and applies an optimal hyper-plane in the mapped space, which provides a better discrimination among classes [10]. Therefore multi-class Support Vector Machine algorithm is proposed for this system. However the selection of suitable kernel function is based on trial and error, therefore after testing different kernels, the Radial Basis Function (RBF), in equation 1, gives the best accuracy results. Where x_i is the training set, x_j is the label set, and γ is the kernel parameter.

$$K\left(x_i, x_j\right) = \exp\left(-\gamma \left\| x_i - x_j \right\|^2\right) \quad , \gamma > 0 \qquad (1)$$

III. HARDWARE IMPLEMENTATION

The Feature Extraction Unit of this system is implemented using the Hardware Descriptive Language (VHDL), as it provides a better hardware optimization, higher speed of operation, lower power consumption, and smaller size compared to any hardware running with a general purpose processors. ModelSim is used in all Pre-routing simulations. After testing the hardware with different data lengths, a general consideration is decided, 32 bit data length is the minimum bit size to achieve high accuracy results. The Classifier Unit is not implemented in this paper however it is tested using the features extracted from this implementation.

A. Wavelet Packet Transform Unit

According to the proposed Wavelet Packet Transform tree in figure 4, an implementation of 19 filter pair is required to acquire the necessary coefficients representing each sub-band. For a second order filter illustrated in figure 5, two 32-bit multipliers and one 64 bit adder are implemented, followed by a truncation unit to maintain the data length at 32 bits; where $h(n)$ represents the filter coefficients, and $x(n)$ represents the EEG input stream.
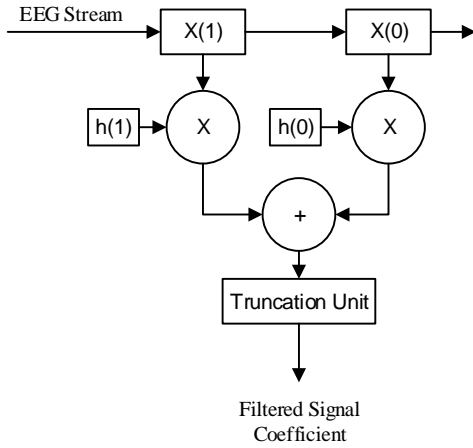

Figure 5: 2nd Order Filter Implementation

Implementing 19 filter pair is nearly impossible as it will require high hardware complexity and large size. Therefore a different approach is implemented. Only one single filter pair is implemented at the core of the WPT with additional circuitry to manage the data flow as illustrated in figure 6.
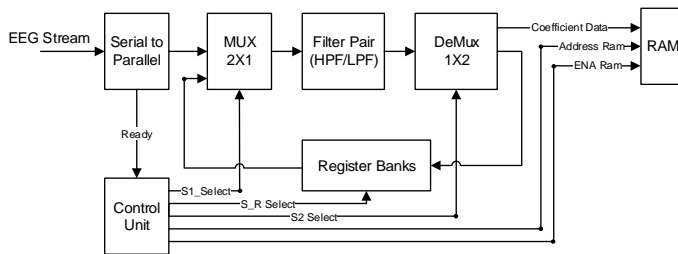

Figure 6: Wavelet Packet Transform Implementation

The design benefits from the time needed to receive each new data point from the stream, by applying further decomposition to values previously decomposed and stored in the Register Banks. The Register Banks Unit holds 36 registers, a pair for each decomposition point in figure 4 (C1, C2, C3, C4, C7, C8, C9, C10, C11, C12, C13, C14, C15, C19, C20, C21, C24, C29). The two Coefficients C6 and C37 are discarded as their values are not needed, while the desired coefficients such as (C5, C16, C17, C18, etc.) are redirected to the 179.25 KB RAM unit to be stored for further processing.

The Control Unit, manages the data flow, and the timing in order to properly map each extracted value to its proper coefficient. Figure 7 demonstrates a partial work plan for the Control Unit.
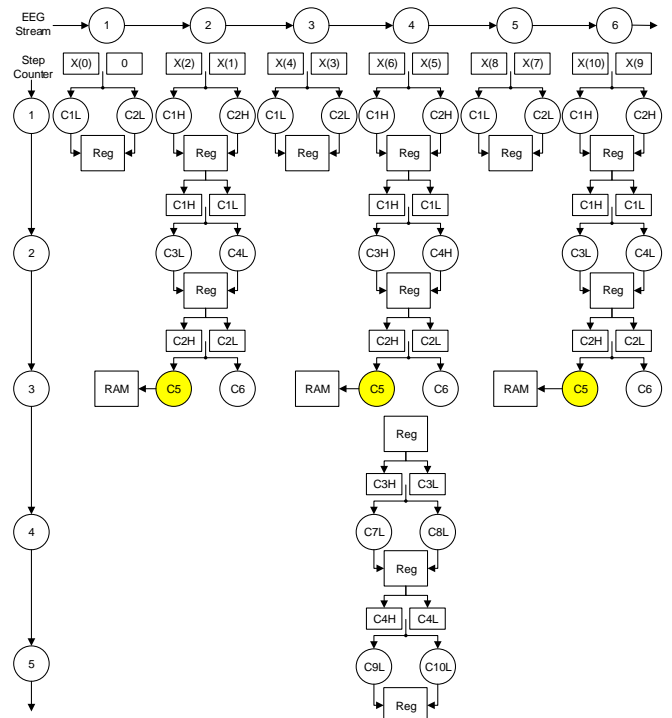

Figure 7: Control Unit Partial Work Plan

B. Feature Calculation Unit

Having all the relevant coefficients ready, the features are calculating using an arithmetic logic unit specifically designed to suit the needs of the system as demonstrated in figure 8. A control unit is implemented to manage the data flow, and a 1.375 KB RAM unit is implemented to store the extracted features.
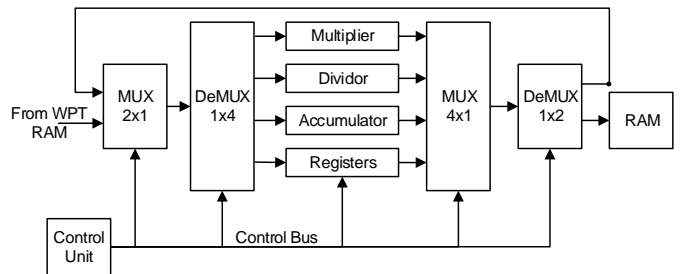

Figure 8: Feature Calculation Unit Implementation

IV. SIMULATION AND RESULTS

Each one of the main blocks undergoes two simulation processes; a software simulation to prove the concept and a pre-routing simulation of the VHDL implementation.

A. Wavelet Packet Transform

The filters being the WPT core, are tested using two set of input data to determine its accuracy. Both software and hardware simulations are conducted. Figure 9 illustrates the hardware pre-routing simulation of the filter pair, while table 2 discusses the verification of pre-routing output values with the software simulation results. POH and POL represents the filter inputs $X(1)$ and $X(0)$ respectively, while the HPF and LPF signals represents the filter outputs.
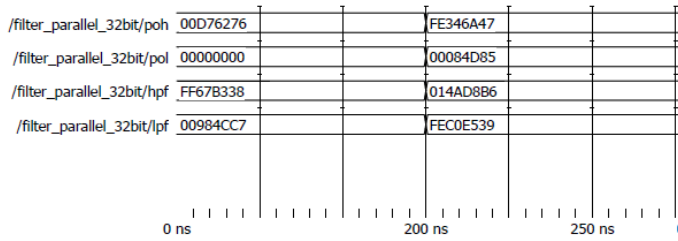
Figure 9: Filter Pair Pre-routing Simulation

TABLE II.   FILTER PAIR OUTPUT

		Pre-routing Results	Software Results	Error %
Data Set1	HPF	-4.7593722343	-4.759372565678690	6.954E-6%
	LPF	4.7593722343	4.759372565678690	6.954E-6%
Data Set2	HPF	10.3389539719	10.338954462404040	4.739E-6%
	LPF	-9.9720182419	-9.972018709041048	4.693E-6%

The WPT Unit is tested using a stream of data forming one complete epoch. Figure 10 demonstrates the operation of this unit.
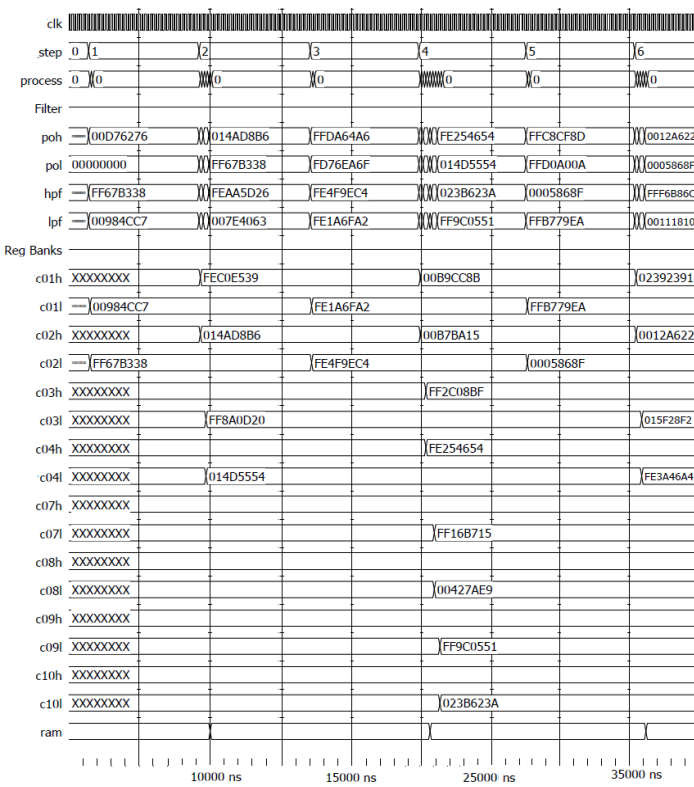

Figure 10: WPT Pre-routing Simulation

Figure 11 represents the average percentage of error calculated for each band separately, S1 to S6 represents the six bands Delta, Theta, Alpha, Spindle, Beta1, and Beta1 respectively. Highest percentage of error is between 8E-5 and 9E-5.
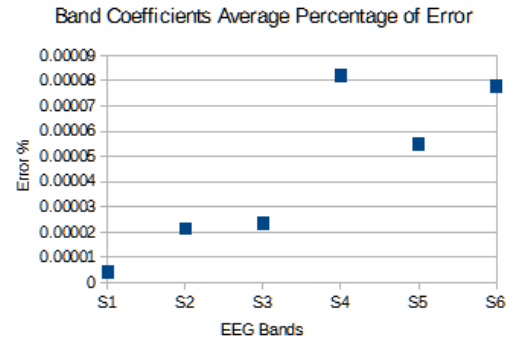

Figure 11: Average Coefficients Error Percentage in Each Band

B. Feature Calculation Unit

The feature calculation unit is simulated by using the coefficient values extracted in the WPT Unit. Figure 12 illustrates a part of this simulation where the marked value is the first feature to be calculated. Average percentage of error in all features is found to be 0.0521%, with the maximum error value at 0.1618%.
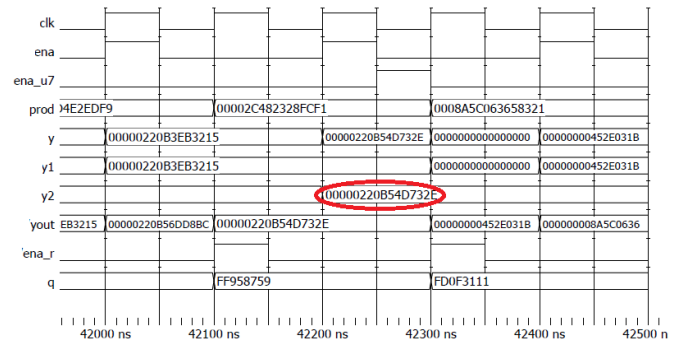

Figure 12: Average Feature Error percentage in an epoch

V. CONCLUSION

The proposed design consists of a Feature Extraction Unit and a Classifier Unit. In this paper, a proposed design for the system was introduced using WPT for the Feature Extraction Unit and SVM for the Classifier Unit. However in this paper only the Feature Extraction Unit was implemented using VHDL.

The Feature Extraction Unit is simulated using a number of healthy and narcoleptic EEG recording, and was achieving a maximum error percentage of 0.1618%.

The SVM algorithm proposed for the system was simulated in MATLAB tool using the features extracted by the hardware implemented and achieved an accuracy rate of 91.47%.

The proposed design which achieves a high level of accuracy, is able to help narcoleptic patients to overcome the drawbacks of the conventional process conducted at sleep clinics. The logging of the results stored within the system provides enough data for the physicians to adjust the medication.

Furthermore, this implementation provides a fully functional hardware that is optimized for the proposed design, while in previous implementations, general purpose processors, were

978

used running a computer program. An optimized hardware implementation results in a faster system with less power consumption, size and system complexity.

Unlike previous devices, a total number of 22 features are extracted instead of just the basic 4 bands – alpha, beta, theta, and delta – proposed in the earlier implementations, providing a better view of the EEG spectrum.

Implementation of the SVM classifier is the future work that will ensure the development of a complete, accurate, portable, and easy to use system.

REFERENCES

[1] Rechtschaffen A. Kales A. "A Manual of Standardized Terminology, Techniques and Scoring System for Sleep Stages of Human Subjects" Los Angeles: Brain Information service/Brain Research Institute, 1968.

[2] "Automatic Sleep Stage Classification Based on EEG Signals by Using Neural Networks and Wavelet Packet Coefficients" 30th Annual International Conference of the IEEE Engineering in Medicine and Biology Society EMBC, 2008.

[3] S. R. I. Gabran, S. Zhang, M. M. A. Salama, R. R. Mansour, C. George "Real-Time Automated Neural-Network Sleep Classifier Using Single Channel EEG Recording for Detection of Narcolepsy Episodes", 30th Annual International Conference of the IEEE Engineering in Medicine and Biology Society EMBC, 2008.

[4] S. R. I. Gabran, W. W. Moussa, M. M. A. Salama "Portable Real-Time Support-Vector-Machine-Based Automated Diagnosis and Detection Device of Narcolepsy Episodes" 31st Annual International Conference of the IEEE EMBS, 2009.

[5] Carskadon, Mary A., and Allan Rechtschaffen. "Monitoring and staging human sleep" Principles and practice of sleep medicine 3, 2000.

[6] Subasi, Abdulhamit. "Automatic recognition of alertness level from EEG by using neural network and wavelet coefficients" *Expert Systems with Applications* 28, no. 4, 2005.

[7] Kiymik, M. Kemal, Mehmet Akin, and Abdulhamit Subasi. "Automatic recognition of alertness level by using wavelet transform and artificial neural network" *Journal of neuroscience methods* 139, no. 2, 2004

[8] Ting, Wu, et al. "EEG feature extraction based on wavelet packet decomposition for brain computer interface" Measurement 41, no. 6, 2008

[9] Wang, Deng, Duoqian Miao, and Chen Xie. "Best basis-based wavelet packet entropy feature extraction and hierarchical EEG classification for epileptic detection" *Expert Systems with Applications* 38, no. 11, 2011

[10] Fatma Guler, N., Elif Derya Ubeyli. "Multiclass support vector machines for EEG-signals classification" Information Technology in Biomedicine, IEEE Transactions 11, no. 2, 2007