A Fast Power Efficient Equalization-Based Digital Background Calibration Technique for Pipelined ADC

Nahla T. Abou-El-Kheir, Mohammed Essam Khedr
Electronics and Communications Department
Arab Academy for Science and Technology
Alexandria, Egypt
nahla.abouelkheir@aast.edu and khedr@aast.edu

Mohamed Abbas
Electrical Engineering Department
Faculty of Engineering, Assiut University
Assiut, Egypt
m-abbas@aun.edu.eg

***Abstract*—A signed variable step size least mean squares (SVSS-LMS) technique is used to boost the convergence rate of digital background calibration for pipelined analog-to-digital converters (ADC). The technique is used to compensate for most known errors, including nonlinear OpAmp gain imperfections, capacitor mismatch and comparator offset. A 12-bit ADC Simulink model is established to verify the technique. Convergence occurs after 5.8K cycle with 42% enhancement over fixed step size LMS. A 22.6% power reduction is achieved as a result of calculation reduction. The proposed technique exhibits improvements in peak DNL from 1 to 0.7 LSB and INL from 33.2 to 2.3 LSB. At a frequency of 100 Msample/s, both SFDR and SNDR reveal noticeable enhancements from 41.6 to 83.1 dB and from 39 to 68.6dB respectively.**

***Keywords*—pipelined analog-to-digital converters; background calibration; least mean squares; variable step size**

I. INTRODUCTION

With the rapid increase in the sampling rate, performance and complexity of portable devices, power reduction has become today's number one target. Digital designs benefit from technology scaling that causes significant power and area reduction. In contrast, their analog counterparts have been struggling to maintain their performance at reasonable power dissipation [1]. Scaling makes power-mismatch and power-linearity tradeoffs more challenging in analog circuits. As, capacitor mismatch is inversely proportional to the capacitor's area and the intrinsic gain drops with scaling, demanding more complicated power-hungry circuits [2]. Consequently, digital help is needed to relax the analog circuits' specifications as well as to make use of technology scaling. The digital assisting circuits are not considered as power overhead on the design itself, as digital low power techniques can be easily implemented to reduce their consumed power [3].

Pipelined analog-to-digital converter (ADC) offers an attractive combination of speed (up to hundreds of Msamples/s) and resolution (up to 16-bit), which makes it widely used in nowadays applications. However, at high speeds, it is hard to implement a high resolution pipelined ADC without calibration [4]. Factors such as capacitor mismatch, residue gain error and OpAmp nonlinearity obviously deteriorate the ADC performance [5]. Many digital calibration techniques have been suggested in the recent years. They are mainly categorized to: (1) foreground and (2) background calibration. The former has the advantage of fast convergence (only hundreds of iterations) but it has two noticeable drawbacks. First, it can't track errors during operation process because it is done offline. Second, it interrupts regular ADC process to apply calibration signal, which is a costly penalty in high speed applications [6]. In contrary, background calibration takes place online during conversion. This property allows continuous system monitoring without interruption and enables tracking of slow environmental variations caused by temperature, supply voltage drifts and device aging [7].

Background calibration can be implemented with the aid of a slow but accurate ADC in parallel with the ADC under calibration as illustrated in Fig. 1 [8]. Gradient descent algorithm is utilized to estimate the tap weight values which are not known a priori due to system errors [9]. This approach can be further enhanced by using signed variable step size (SVSS) LMS (Least mean squares) technique to speed up the system convergence [10]. SVSS technique has the ability to track slowly varying errors efficiently with low complexity and power overhead compared to other techniques such as variable step size (VSS) and modified variable step size (MVSS) methods [11, 12].

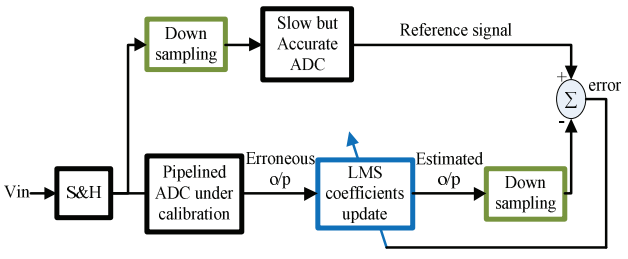

Fig. 1. Background calibration using parallel slow but accurate ADC

In this paper, SVSS-LMS based digital calibration technique is applied to a 12-bit pipelined ADC; composed of twelve1.5-bit stages and a 2-bit flash. The technique aims to

compensate for capacitor mismatch, comparator offset and both linear and nonlinear OpAmp imperfections with the least complexity and power consumption. This technique has the advantage of spending less power in analog circuitry especially in the reference ADC. Since, it works on decreasing the sampling rate of the reference ADC, by increasing the decimation factor.

The rest of the paper is organized as follows. In section II, Equalization-based digital calibration scheme is explained. The SVSS LMS algorithm is presented in section III. In section IV, simulation results are discussed. Finally some conclusions are drawn in section V.

II. EQUALIZATION-BASED DIGITAL CALIBRATION

Equalization-based calibration scheme is known for its high convergence rate compared to statistical-based and correlation-based methods [13]. As illustrated in Fig. 1, the process starts when the output of the pipeline ADC under calibration is fed to LMS adaptive filter (ADF) to compensate for the ADC errors and generate an estimated digital output. Subsequently, the estimated output is compared to the reference signal coming from the accurate ADC. Next, their difference (the error) is provided back again to the ADF. Finally, the ADF updates the coefficients based on LMS algorithm, to be able to track errors, and so forth.

The code domain representation of 1.5-bit/stage MDAC transfer characteristics is elaborated next. Afterwards, it is generalized to include multi-stage pipelined ADC code formulation.

A. Flip-Around MDAC Architecture

As shown in Fig. 2, this paper deploys flip-around multiplying digital to analog converter (MDAC) 1.5-bit/stage architecture. It is commonly used because of its low complexity and good immunity to comparator offset [8] and DAC errors, which is more significant in higher bit per stage architectures [3].

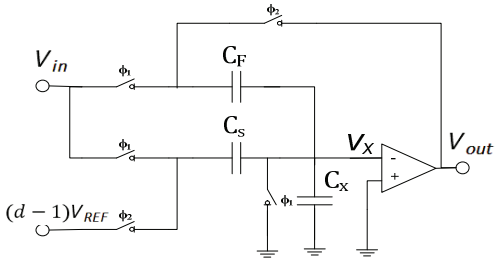

Fig. 2. 1.5 bit/stage MDAC architecture

The nonlinearities introduced by the OpAmp gain can be assumed to be memoryless and weakly non-linear functions of the input. Hence, they can be modeled using Taylor's expansion [5]. Moreover, for a fully differential amplifier the even polynomials of the expansion can be neglected [14]. In this paper only the 3rd and 5th order nonlinearities are considered in the OpAmp open loop transfer function as follows:

$$V_{out} \approx A_o(V_X + \gamma_3 V_X^3 + \gamma_5 V_X^5) \quad (1)$$

where, A_o is the opamp DC gain, V_X is its input voltage, and γ_3 and γ_5 are the third and fifth nonlinearity coefficients. If the OpAmp is placed in a feedback circuit the input (V_X) can be approximated by:

$$V_X \approx \varepsilon_1 V_{out} + \varepsilon_3 V_{out}^3 + \varepsilon_5 V_{out}^5 \quad (2)$$

where $\varepsilon_1 = \frac{1}{A_o}$, $\varepsilon_3 = \frac{\gamma_3}{{A_o}^3}$, and $\varepsilon_5 = \frac{3\gamma_3^2 - \gamma_5}{{A_o}^5}$.

By applying previous OpAmp equations to MDAC general equation derived from charge conservation in sampling and hold mode of operation, we get the following equations:

$$V_{out} = \frac{C_F + C_S}{C_F + (C_F + C_S + C_X)/A_o(V_{out})} V_{in} - \frac{C_S}{C_F + (C_F + C_S + C_X)/A_o(V_{out})}(d-1)V_{REF} \quad (3)$$

where,

$$A_o(V_{out}) = \frac{1}{\varepsilon_1 + \varepsilon_3 V_{out}^2 + \varepsilon_5 V_{out}^4} \quad (4)$$

V_{out} is the residue voltage, C_F is the feedback capacitor, C_S is the sampling capacitor, C_X is the parasitic capacitor, d is the sub-ADC output taking values 0,1 or 2, V_{REF} is the reference voltage and $A_o(V_{out})$ is the nonlinear OpAmp gain.

B. Code Domain Transfer Characteristics

The transfer characteristics per stage are represented as code domain finite impulse response (FIR) formula to facilitate the coefficients update done by the LMS ADF. After dividing (3) by V_{REF} we reach the following digital representation:

$$D_{in} = D_{out}\alpha_1 + D_{out}^3\alpha_3 + D_{out}^5\alpha_5 + (d-1)\beta \quad (5)$$

where, $D_{in} = \frac{V_{in}}{V_{REF}}$, $D_{out} = \frac{V_{out}}{V_{REF}}$, $\alpha_k = f_k(C_S, C_F, C_x, A(D_{out}))$ and $\beta = (\frac{C_S}{C_F + C_S})$. In an ideal ADC, α_1 and β are equal to 0.5, and α_3 and α_5 are equal to zero.

For the k[th] stage in pipelined ADC, its output (residue) is the next stage's input in the analog domain. Consequently their digital representation is said to be equal ($D_{o,K} = D_{in,k+1}$). Therefore, we can express the input for multi-stage pipelined ADC as follows:

$$D_{in} = D_{in,2}\alpha_{1,1} + D_{in,2}^3\alpha_{1,3} + D_{in,2}^5\alpha_{1,5} + (d_1 - 1)\beta_1 \quad (6)$$

where, $D_{in,2}$ is obtained from previous stages and so on, such that:

$$D_{in,k} = D_{in,k+1}\alpha_{k,1} + D_{in,k+1}^3\alpha_{k,3} + D_{in,k+1}^5\alpha_{k,5} + (d_k - 1)\beta_k \quad (7)$$

Eq. (6) proves that the first stage input D_{in} can be obtained from the summation of weighted stage input polynomials and weighted sub-ADC outputs. Accordingly, this is the key factor of the proposed calibration technique presented in the next section.

III. Proposed Adaptation Method

As previously mentioned, the proposed calibration technique makes use of the redundancy between the pipelined stages to correct the final ADC output. Fig. 3 shows the proposed technique used to correct the errors in a 12-bit pipelined ADC. The summation of digital outputs coming from the backend stages is used to correct the errors in early stages with the help of the ADF. The mechanism of weight updating in ADF is demonstrated in this section.

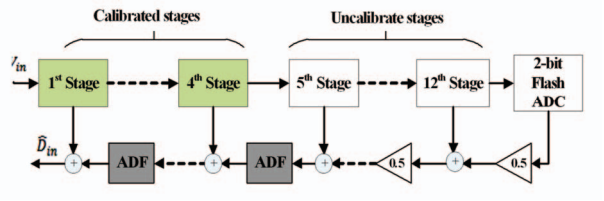

Fig. 3. The proposed calibration technique

A. LMS Algorithm

As declared in the previous section, to estimate the k-stage input ($D_{in,k}$), digital inputs of higher order ($D_{in,k+1}$, ..) stages are needed. Therefore, the calibration is performed from the backend to the front stages. Accordingly, the ADF coefficients converge similarly from last to first stage. At each iteration the total estimated input signal ($\widehat{D}_{in}$) is compared to the reference signal to calculate the error. Each kth stage's ADF has three inputs: previous stage estimate ($D_{in,k+1}$), its sub-ADC output (d_k) and the error (e). For the first two stages, a 4-tap ADF is implemented whereas in the 3rd and the 4th stages only two taps per stage are necessary as pointed out in (7). The four filters estimate the coefficients as pointed out in the previous section. The LMS technique is responsible of updating these coefficients with the aid of the three inputs and the step size (μ). Eq. (8) shows an example of weight update based on LMS at the nth iteration:

$$\alpha(n+1) = \alpha(n) + \mu(n)e(n)D_{in,k+1}(n) \tag{8}$$

B. Variable Step Size

The proposed technique uses SVSS algorithm to speed up the convergence while maintaining a low steady state error. Some VSS algorithms have higher complexity, which may reach six extra multiplications per iteration more than normal LMS [13]. To optimize the convergence rate and power consumption, this paper exploits SVSS algorithm. Eq. (9) displays the way the step size fluctuates with the error sign, constant forgetting factor (θ) and the small constant (ρ) [11]

$$\grave{\mu}(n) = \theta\mu(n-1) + \rho sign(e(n-1)) \tag{9}$$

where θ and ρ are constants that range from 0 to 1. Also, the step size is bounded by:

$$\mu(n) = \begin{cases} \mu_{max} & if \grave{\mu}(n) > \mu_{max} \\ \mu_{min} & if \grave{\mu}(n) < \mu_{min} \\ \grave{\mu}(n) & otherwise \end{cases} \tag{10}$$

and μ_{max} must satisfy the LMS convergence criteria that depends on the maximum eigen value (λ_{max}) presented by:

$$0 < E\{\mu_{max}\} < \frac{2}{\lambda_{max}} \tag{11}$$

Initially, the step size is adjusted close to μ_{max} to ensure fast convergence at the beginning and then it decreases to reach $\mu_{min}$to grantee low steady state error. $\mu_{min}$is usually chosen close to the fixed step size. This algorithm is proven to be effective in environments where the error is considered to be slowly varying which is our case in pipelined ADC.

The normal LMS and SVSS-LMS complexity can be measured by the number of multiplications per iteration. The former method requires only $3M$ multiplications per iteration when each tap has a different step size, where M is the number of taps. The latter deploys $4M$ multiplications per iteration. Accordingly, to implement the four ADF 48 multiplications per iteration are needed by SVSS based algorithm while only 36 multiplications are needed by the FSS based. Although, the SVSS appear to have higher complexity, it will eventually pay-off as concluded in the coming section.

IV. Simulation Results

A 12-bit pipelined ADC Simulink model is developed to evaluate the proposed technique. OpAmp nonlinearities up to the 5th order besides linear errors including finite gain, capacitor mismatch, parasitic capacitor effect and comparator offset are corrected in the first two stages. However, the third and fourth stages are corrected only for linear errors. Finite gain of 53, capacitor mismatch error of 5%, parasitic capacitor error of 30% and a 10%V_{REF} comparator offset error are introduced in all stages. The OpAmp open loop nonlinear gain curve is modeled as presented in Fig. 4.

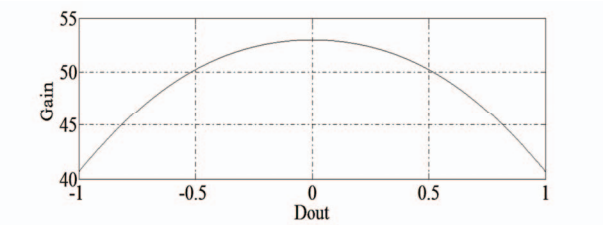

Fig. 4. OpAmp nonlinear gain model

Although, the errors were introduced in all stages, only four ADF units were sufficient to achieve ≃ 12 bits accuracy. As manifested in Fig. 5, as the number of calibrated stages increase the Dynamic parameters improves while the complexity increases. The step sizes of different ADF were adjusted so that the 4th stage converges first then the 3rd stage and so on. For instance, the 1st stage's lowest μ_{min} is set to 2^{-9} while the 4th stage's lowest μ_{min} is set to 2^{-4}. Moreover, The SVSS parameters in the four stages are adjusted to $\theta = 0.995$ and $\rho = 1e-7$.

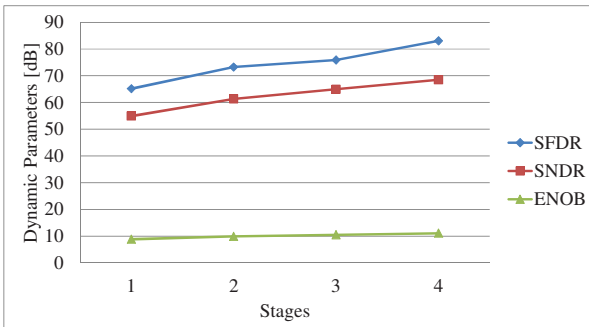

Fig. 5. Dynamic parameters vs stages calibrated

The mean square error (MSE) is calculated for both SVSS and fixed step size (FSS) to predict the learning curve. As seen in Fig. 6, the convergence rate of SVSS which is 5.8K cycles is approximately double that of the FSS which converges after 10K cycle. That means that the SVSS needs 278.4K multiplications to reach steady state whereas, the FSS needs 360K multiplications. Hereafter, the proposed technique is capable of reducing the total number of calculations by 22.6%. Thus, reducing the power consumed in calculations and the power spent in the slow but accurate ADC operation; the decimation factor can be decreased to meet the same time requirement. As, the filter adaptation rate which is controlled by the decimation factor, is the conversion rate of the reference ADC. For instance, if a decimation factor of value 1000 is used the conversion rate of the reference ADC should be $f_s/1000$.

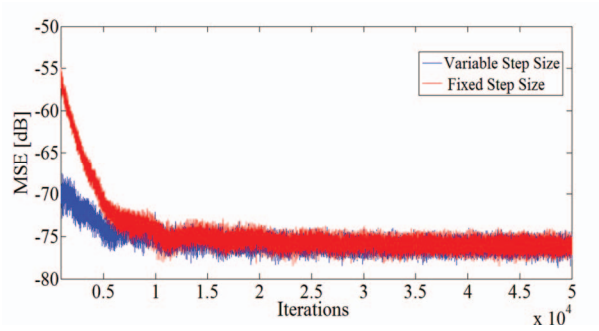

Fig. 6. Learning curve of variable step size vs fixed step size

The dynamic parameters are measured at f_s=100Msample/s and f_{in}=9.99 MHz. the results are summarized in Table I.

TABLE I.
DYNAMIC RESULTS

Dynamic Parameters	*Before calibration*	*After calibration*
SFDR	41.6dB	83.1dB
SNDR	39 dB	68.6dB

The table shows the SFDR and SNDR enhancements from 41.6dB to 83.1dB and from 39dB to 68.6dB respectively. After calibration, the calculated ENOB is 11.1dB. The power spectral density (PSD) is presented in Fig. 7, it can be observed how harmonics are corrected using this technique. The DC measurements were also measured, no missing codes were found in the estimated input ($\widehat{D}_{in}$). The peak DNL before and after the calibration are 1/0.7 LSB and the peak INL before and after calibration are 33.2/2.3 LSB.

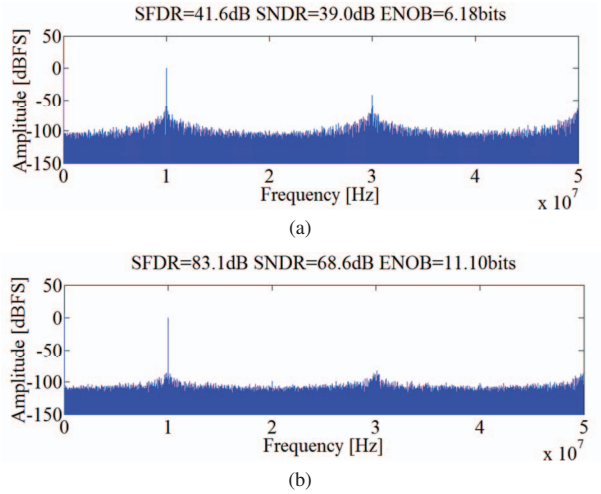

Fig. 7. Frequency spectrum at f_s=100 Msample/s and f_{in}=9.99 MHz (a) before calibration, (b) after calibration

V. CONCLUSION

A fast digital calibration employing SVSS-LMS algorithm is investigated in this paper. This technique targets fast convergence with low complexity and hence power consumption. The technique is applied to a 12-bit ADC where linear and nonlinear errors up to 5th order were calibrated for the first two stages and only linear errors were calibrated for the rest. Only the first four stages need calibration, so that the steady state error reaches ≃ 12-bit accuracy. The technique is implemented using Simulink and it is compared to its FSS-LMS based counterpart. With a sine wave input having a frequency of f_{in}=9.99 MHz sampled at a rate of 100 Msample/s, the system convergence is observed after 5.8K cycles. Hence, it is considered 42% faster than FSS-LMS based technique. Therefore, the proposed technique is capable of saving up to 22.6% of the power consumed in calculations. Hence, relax the reference ADC requirements by decreasing its conversion rate and reduce the power spent in it. Moreover, the results indicate 42dB and 30dB improvements in SFDR and SNDR respectively.

REFERENCES

[1] B. Murmann and B.E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," Journal of Solid-State Circuits, vol.38, pp. 2040-2050, Dec. 2003.

[2] I. Ahmed, and D. A. Johns, "An 11-Bit 45 MS/s Pipelined ADC With Rapid Calibration of DAC Errors in a Multibit Pipeline Stage," IEEE Journal of Solid-State Circuits, vol. 43, pp.1626-1636, July 2008.

[3] N. T. Abou-El-Kheir, M. S. El-Kharashi and M. A. El-Moursy, "A Low Power Programmable FIR Filter using Sharing Multiplication Technique," IEEE International Conference on IC Design & Technology, June 2012.

[4] L. Shi, W. Zhao, J. Wu, and C. Chen, "Digital Background Calibration Techniques for Pipelined ADC Based on Comparator Dithering," IEEE Transactions on Circuits and Systems II: Express Briefs, pp. 239-243, April 2012.

[5] B. D. Sahoo, B. Razavi, "A 12-Bit 200-MHz CMOS ADC", Journal of Solid-State Circuits, vol. 44, pp. 2366-2380, Sept. 2009.

[6] Y. Chiu, C. W. Tsang, B, Nikolic, and Paul R. Gray, "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters," IEEE Transactios on Circuits And Systems, vol. 51, pp. 38-46, Jan. 2004.

[7] B. J. Farahani abd A.Mervua, " Low Power High Performance Digitally Assited pipelined ADC," IEEE Computer Soceity Annual Symosium on VLSI, pp. 111-116, April 2008.

[8] U. Moon and B. S. Song, "Background digital calibration techniques for pipelined ADC's," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 44, pp. 102–109, Feb. 1997.

[9] S. S. Haykin, Adaptive Filter Theory, 3rd ed. Upper Saddle River, NJ: Prentice-Hall, 1996.

[10] T. I. Haweel," A simple variable step size LMS adaptive algorithm," International Journal of Circuit Theory And Applications, vol. 32, pp. 523-536, Nov. 2004.

[11] R. H. Kwong, and E. W. Johnston, "A Variable Step Size LMS Algorithm," IEEE Transactions on Signal Processing, vol. 40, pp. 1633-1642, July 1992.

[12] T. Aboulnasr, and K. Mayyas, " A Robust Variable Step-Size LMS-Type Algorithm: Analysis and Simulations," IEEE Transactions on Signal Processing, vol. 45, pp. 631-639, March 1997.

[13] C. Tsang, Y. Chiu, J. Vanderhaegen, S. Hoyos, C. Chen, R. Brodersen, and B. Nikoli, "Background ADC Calibration in Digital Domain," IEEE 2008 Custom Intergrated Circuits Conference, pp. 301-304, Sept. 2008.

[14] B. Zeinali, T. Moosazadeh, M. Yavari, and A. Rodriguez-Vazquez, "Equalization-Based Digital Background Calibration Technique for Pipelined ADCs," IEEE Transactios on Very Large Scale Integration Systems, vol. 22 ,pp. 322-333, Feb. 2013.