Performance with Application to Folded Cascode of a Near-Ballistic Limit Carbon Nano Transistor (CNT) Circuits

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ABSRACT: In this paper, we present a performance evaluation and comparison betweeen a short channel MOSFET and a carbon nanotransistors (CNT) operating near the limit of the ballistic transport. The carbon nanotube can be used in both device fabrication and circuit interconnects as a carbon nanowire (CNW). We provide a performance comparison of a cascode amplifier circuit using quasi-analytical circuit compatible model for the intrinsic ballistic CNFET. Analysis and simulation results show that the CNT is superior from the points of view of the gain and the power dissipation, and the superior transfer characteristics.

I. Introduction

Carrier transport in semiconductors follows two main mechanisms: the drift-diffusion and ballistic mechanisms. In the first, the mean free path between collisions or scattering events is much shorter than the MOSFET device channel length ($\lambda << L$). In this case, if the device is operating above threshold region, the drift dominates diffusion. If the device operates below threshold, the diffusion dominates.

Under the above condition, one can ignore scattering completely. In this case, MOSFET operates more like a vacuum tube than a conventional semiconductor device, i.e., a thermionic emission. Modern devices work between drift-diffusion and ballistic regimes. However, drift-diffusion theory is no longer strictly valid, but it actually provides some insights that may be useful when the device dimensions scale down to the submicron range. Three categories of devices are in our concern: the carbon nano field effect transistor, the quasiballistic and the ballistic MOSFET. In this paper, we presnt the performance evaluation for both carbon nanotube and short channel MOSFET operating near the ballistic limit.

In [1], it was shown experimentally that ultra long elastic scattering mean free path of about 1 μm which implies ballistic or near ballistic transport leading to mobilities in the order of 10^3 to 10^4 $cm^2/V.s$. The current carrying capability is in the order of 10^9 A/cm^2 in multiwalled CNTs. This is three orders higher than the maximum current carrying capacity of copper. The above superior carrier transport and conduction characteristic makes it desirable for nanoscale electronic devices and interconnects.

II. Metrics for Performance Evaluation and Comparison of Nanoscale Transistors

As CMOS dimensions scale deeply into the submicron (nano) range, many of the device nonideal behaviors arise. One of these nonidealities is the source drain series resistance contribution to the total resistance of the device. Another metric is the inverter effective drive current that appears to be useful in performance evaluation of nanoscale devices. This current is given by:

$$I_{eff}=1/2[C_{eff}V_{DD}]/\tau pd \quad (1)$$

Where, Ceff is effective oxide capacitance, and τpd is the propagation delay between source and drain terminals. So, it is important to include the nonidealities in the simulation model used . It was shown in [3] that, the four point model of the inverter effective current is the model that is most correlated to the practical device operation. Throughout this paper, the analysis takes into consideration the nonideal behavior of the nanoscale devices, and the four point effective inverter current in addition to the resizing of the nMOS and pMOS aspect ratios to ensure the equality of the rise in fall times for both transistors.

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III. MODEL DESCRIPTION

The model used in this paper is shown in Fig. 1. It is known as the nine capacitance model [2]. In this model, we consider three current sources in the CNFET:

a. The thermionic current contributed by the semiconducting sub-bands (I_{semi}) derived from the classical band theory.
b- The current contributed by the metallic sub-bands (I_{metal}).
c- The leakage current (I_{btbt}) caused by the band-to-band tunneling (BTBT) mechanism through the semiconducting sub-bands.

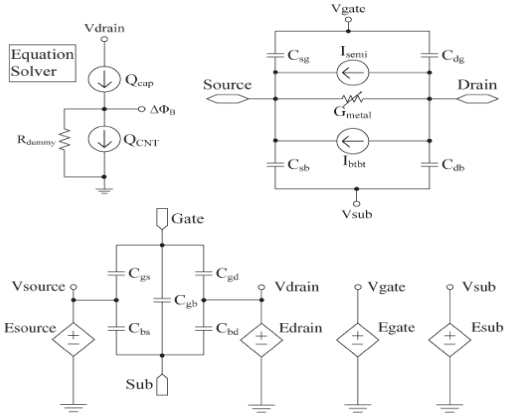

Fig. 1. Circuit model for the CNT [2].

Concerning I_{semi}, for semiconducting subbands, we only consider the electron current for the nFET because the hole current is suppressed by the n-type heavily doped source/drain.

The total current contributed by all substates is equal to the current flowing from the drain to the source (+k branch) minus the current flowing from the source to the drain (−k branch)[3] i.e.,

$$I_{semi}(V_{ch,DS},V_{ch,GS}) = 2\sum_{m=1}^{M}\sum_{l=1}^{L}[T_{LR}J_{m,l}(0,\Delta\Phi_B)|_{+k} - T_{RL}J_{m,l}(V_{ch,DS},\Delta\Phi_B)|_{-k}] \quad (2)$$

where $V_{ch,DS}$ and $V_{ch,GS}$ are the Fermi potential differences near the source side within the channel, ΔΦB is the channel surface-potential change with gate/drain bias, $J_{m,l}$ is the current contributed by the substate (m,l), $T_{L,R}$ and $T_{R,L}$ are the transmission probabilities, the factor of two is due to the double degeneracy of the sub-band, M and L are the numbers of subbands and substates, respectively.

$$Q_{CAP}=Q_{CNT}$$

$$Q_{CNT}=\frac{4e}{L_g}\sum_{m=mo}^{M}\sum_{l=0}^{L}\left[\frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B)/kT}} + \frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B+eV_{DS})/kT}}\right] \quad (3)$$

Concerning I_{metal}, for metallic sub-bands of metallic nanotubes, the current includes both the electron and hole currents, i.e.,

$$I_{metal} = (1-m0)\frac{4e^2}{h}T_{metal}V_{ch,DS} \quad (4)$$

where T_{metal} is the transmission probability, given by

$$T_{metal} = \frac{\lambda_{ap}\lambda_{op}}{\lambda_{ap}\lambda_{op}+(\lambda_{ap}+\lambda_{op}).L_g} \quad (5)$$

where λ_{op} is the optical phonon-scattering wavelength (~15 nm) and λ_{ap} is the acoustic phonon-scattering wave length (~500 nm). It should be noted that in CNFET there exist three mechanisms for scattering [3]. These are the acoustic phonon scattering (near-elastic process), the optical phonon scattering (inelastic process), and the elastic scattering which is considered here to be independent of the carrier energy [2]

Concerning I_{BTBT} and assuming a ballistic transport for the tunneling process, the BTBT current is approximated by the BTBT tunneling probability (T_{BTBT}) times the maximum possible tunneling current integrated from the conduction band at the drain side up to the valance band at the source side, i.e.,

$$I_{BTBT} = \frac{4e}{h}kT.\sum_{m=1}^{M}\left[T_{btbt}\ln\left(\frac{1+e^{\frac{eV_{ch,DS}-E_{m,0}-E_f}{kT}}}{1+e^{\frac{E_{m,0}-E_f}{kT}}}\right)\times \frac{\max(eV_{ch,DS}-2E_{m,0},0)}{eV_{ch,DS}-2E_{m,0}}\right] \quad (6)$$

where T_{BTBT} is the transmission probability, given by

$$T_{BTBT} \approx \frac{\pi^2}{9}\exp\left(-\frac{\pi m^{*\left(\frac{1}{2}\right)}(\eta_m 2E_{m,0})^{\frac{3}{2}}}{2^{\frac{3}{2}}e.\hbar.F}\right) \quad (7)$$

where η_m is a fitting parameter and F is given by:

$$F = (V_{ch,DS} + \frac{(E_f-\Delta\Phi_B)}{e})/l_{relax} \quad (8)$$

Is the electrical field triggering the tunneling process near the drain channel junction. The potential drop across the drain-channel junction is assumed to relax over the distance l_{relax}.

IV. TRANSCAPACITANCE NETWORK

The ac response of the CNFET device can be revealed using a controlled transfer capacitance array in between the source, drain, gate and body[2,4].

$$C_{sg} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot}-2(1-\beta)C_c}{\frac{\partial V_g}{\partial \Delta\Phi_B}}\right) \quad (9)$$

$$C_{dg} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot}-2(\beta)C_c}{\frac{\partial V_g}{\partial \Delta\Phi_B}}\right) \quad (10)$$

$$\frac{\partial V_G}{\partial \Delta\Phi_B} = \frac{1}{eC_{ox}}\left(C_{tot} + C_{Qs} + C_{Qd}\right) \quad (11)$$

$$C_{Qs} = \frac{4e^2}{L_g.kT}\sum_{m=m0}^{M}\sum_{l=0}^{L}\left[\frac{e^{(E_{m,l}-\Delta\Phi_B)/kT}}{\left(1+e^{\frac{E_{m,l}-\Delta\Phi_B}{kT}}\right)^2}\right] \quad (12)$$

With small gate bias (Em,0 >> $\Delta\Phi_B$), the quantum capacitances due to carriers from source (+k branch) and drain (-k branch) are given by:

$$C_{Qd} = \frac{4e^2}{L_g.kT}\sum_{m=m0}^{M}\sum_{l=0}^{L}\left[\frac{e^{(E_{m,l}-\Delta\Phi_B+eV_{ch,DS})/kT}}{\left(1+e^{\frac{E_{m,l}-\Delta\Phi_B+eV_{ch,DS}}{kT}}\right)^2}\right] \quad (13)$$

$$C_{Qs} = \frac{4e^2}{L_g.kT}\sum_{m=m0}^{M}\sum_{l=0}^{L}\left[\frac{e^{(E_{m,l}-\Delta\Phi_B)/kT}}{\left(1+e^{\frac{(E_{m,l}-\Delta\Phi_B)}{kT}}\right)^2}\right] \quad (14)$$

$$C_{sg} = \frac{L_g C_{ox}}{2}\frac{C_{Qs}+C_{Qd}+2(1-\beta)C_c}{C_{tot}+C_{Qs}+C_{Qd}} \quad (15)$$

$$C_{dg} = \frac{L_g C_{ox}}{2}\frac{C_{Qs}+C_{Qd}+2\beta C_c}{C_{tot}+C_{Qs}+C_{Qd}} \quad (16)$$

$$C_{bg} = C_{gb} = \frac{L_g C_{sub} C_{ox}}{C_{tot}+C_{Qs}+C_{Qd}} \quad (17)$$

$$C_{gs} = \frac{L_g C_{ox}[C_{Qs}+(1-\beta)C_c]}{C_{tot}+C_{Qs}+C_{Qd}} \quad (18)$$

$$C_{gd} = \frac{L_g C_{ox}[C_{Qd}+(\beta)C_c]}{C_{tot}+C_{Qs}+C_{Qd}} \quad (19)$$

$$C_{bs} = C_{gs}\frac{C_{sub}}{C_{ox}} \quad (20)$$

$$C_{bd} = C_{gd}\frac{C_{sub}}{C_{ox}} \quad (21)$$

V. CMOS MODEL EQUATIONS

The long channel MOSFET small signal model including the inter electrode capacitances is shown in Fig.2 [5].

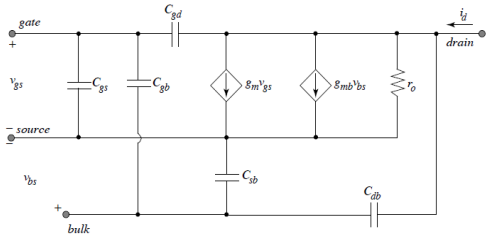

Fig. 2. Small-signal MOS transistor equivalent circuit [5].

The device transconductance is given by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = k'\frac{W}{L}(V_{GS}-V_t)(1+\lambda V_{DS}) \quad (22)$$

$$i_d = I_d - I_D = k'\frac{W}{L}(V_{GS}-V_t)v_i\left[1+\frac{v_i}{2(V_{GS}-V_t)}\right] \quad (23)$$

Due to device symmetry,

$$C_{gs} = C_{gd} = \frac{C_{ox}WL}{2} \quad (24)$$

$$\frac{\Delta V_{DS}}{\Delta I_D} = \frac{V_A}{I_D} = \frac{1}{\lambda I_D} = r_o \quad (25)$$

where V_A is the Early voltage. Taking the body effect into consideration, the transconductance due to body effect is given by:

$$g_{mb} = \frac{\gamma k'\left(\frac{W}{L}\right)(V_{GS}-V_t)(1+\lambda V_{DS})}{2\sqrt{2\Phi_f+V_{SB}}} \quad (26)$$

$$C_{sb} = \frac{C_{sb0}}{\left(1+\frac{V_{SB}}{\Psi_0}\right)^{1/2}} \quad (27)$$

$$C_{db} = \frac{C_{db0}}{\left(1+\frac{V_{DB}}{\Psi_0}\right)^{1/2}} \quad (28)$$

Where, γ is the Body effect coefficient, λ is the channel length modulation coefficient, v_t is the threshold voltage, $\Psi_0$is the built-in potential, Φ_f is the Fermi-potential, C_{sb0}, C_{db0}, are the source and drain capacitances when the source or drain are tied to the body [6].

VI. RESULTS AND DISCUSSION

The described model was used to simulate the folded cascode amplifier circuit [6], Fig. 3.

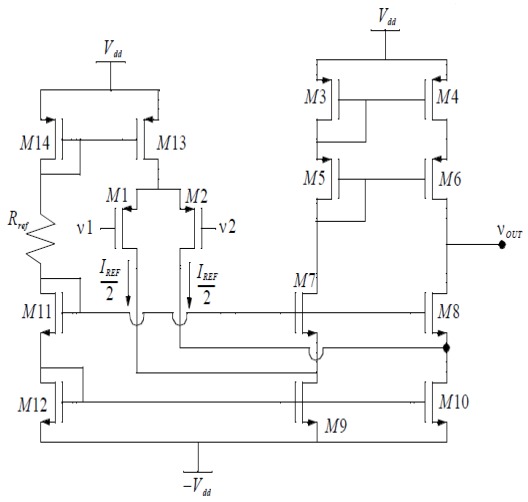

Fig 3. Folded Cascode Amplifier Circuit

We summarize the simulation results in TABLE I.

TABLE I COMPARISON OF THE PERFORMANCE OF FOLDED CASCODE REALIZED BY CMOS AND CNFET

Parameter	CMOS 180nm	CNFET 32nm
Power dissipation	113.578µW	16.65µW
Gain	289.32	1.33*10^6
Input Resistance	1.0*10^20Ω	5.0*10^11Ω
Output Resistance	1.413*10^6Ω	3.681*10^10 Ω
Output Noise	28.56mV	0.37mV
Swing	3.62V	1.82V

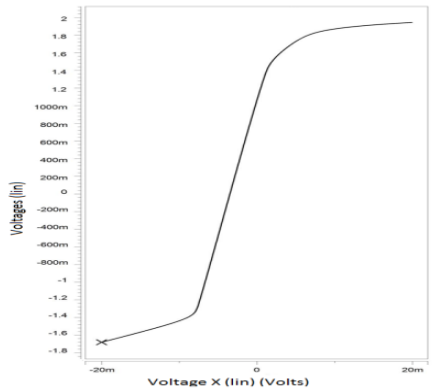

Fig 4. Transfer function (folded cascode CMOS 180nm)

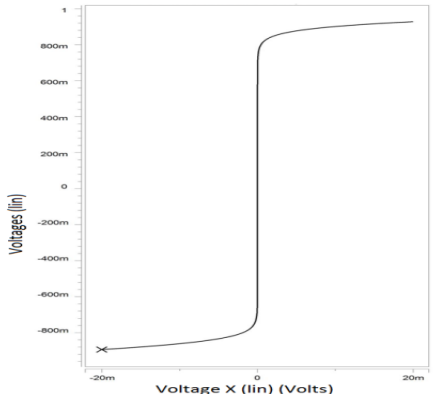

Fig 5. Transfer function (folded cascode CNFET 32nm)

VI. CONCLUSION

In this paper, we provided a quasi-analytical circuit compatible model for intrinsic ballistic CNFET. This model is seen to be very effective for various CNFET structures with a wide range of bias conditions and non ideal effects. This can be used in conventional circuit simulators. We also conclude that, the CNFET enhancement over the normal MOSFET manifests itself in the gain and the power dissipation, and the superior transfer characteristics. It must be noted that smaller V_{DD} bias was used for the CNFET than the CMOS, explaining the lower swing.

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