A CCII -Amplifier for High-Gain and High Bandwidth Outdoor WOC Applications

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Abstract— **This work presents a method for solving an outdoor wireless communications (WOC) receiving problem. A class II current conveyor (CCII) is designed and simulated under a wide range of operating conditions. Effects on bandwidth and input impedance are simulated and compared with previously designed architectures resulting in a better amplification performance. The design affecting parameters are investigated including: photodiode internal capacitance, control feedback resistance, resistive and capacitive loads, temperature, input and output noise levels. OrCAD 10.5 is used as a simulation tool.**

Index Terms—**Class II current conveyor, Control feedback technique, Equivalent input current noise level, Photodiode internal capacitance, Wireless optical communication.**

I. INTRODUCTION

Infrared free-space optical receivers find applications in laptop computers, cellular phones, digital cameras, computer peripherals, personal digital assistants and many other consumer electronics equipped with a short-distance infrared communication port. In infrared wireless optical receivers, the use of a sensitive current-input preamplifier or buffer to process the signal current from the photodiode is essential. Infrared wireless preamplifiers or buffer require a wide bandwidth, a wide dynamic range and the ability to reject ambient light. According to Infrared Data Association (IrDA), data rates of 100 Mb/s and higher are now being investigated [1], [2].

An example of those are high-speed optical air links developed, using low cost photodiodes attached to CMOS-based transimpedance front-ends [3], [4]. This system is an example of an outdoor WOC problem. These are situations when low current, high bandwidths signals should be able to go through large capacitance nodes. But, the capacitive load in these nodes severely restricts overall system bandwidth [5-7]. A novel class II current amplifier was introduced in [8] and used effectively as a technique in [8], [9] to answer this problem. This amplifier uses class-II Current Conveyor concepts (CCII) to implement a controlled low input impedance system. Using this amplifier decreases the need of a transimpedance amplifier for an outdoor WOC application.

In this paper, we are going to use the CCII amplifier introduced with modifications to solve the previously discussed problem and improve the performance for fast Ethernet line-of-sight optical links. The following sections introduce the mathematical and theoretical information about CCII based cell in: modeling scheme, input impedance control and effective input dynamic range. The theoretical background with the used diagram for CCII buffer is followed by simulation and discussion.

II. THEORETICAL AND MATHMATICAL BACKGROUND

A. *Modeling of CCII*

A second generation current conveyor block diagram CCII in introduced in Fig. 1.

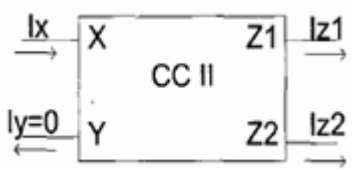

Fig. 1 Second generation current conveyor basic cell [8].

This diagram can be adequately described by the following matrix equation [8]:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{pmatrix} g_y & 0 & 0 \\ A_v & r_x & 0 \\ 0 & A_i & g_z \end{pmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \qquad (1)$$

The elements inside the system matrix represent the relevant parameters of the current conveyor which are frequency dependent. A_V represents the voltage gain between the input nodes X and Y and A_i represents the current gain between the X input and one generic Z output. In order to include both the effects of the inputs (X and Y) and the output (Z), the system matrix takes into account the impedances (admittances) at ports X, Y and Z. High frequency effect should be taken in consideration through all procedures [8].

B. *Input Impedance Control*

CCII input impedance (R_{in}) can be controlled by the circuit depicted in Fig. 2. This figure includes the basic CCII cell attached to circuits that can specify operation of the amplifier.

Attached circuits include a model for the input photodiode (I_{in} and C_{pin} are the photocurrent and photodiode capacitance), pad interconnections (C_{by} is a bypass capacitor), feedback control resistance (R_{comp}), and amplifier load (R_{out} and C_{out}) [8].

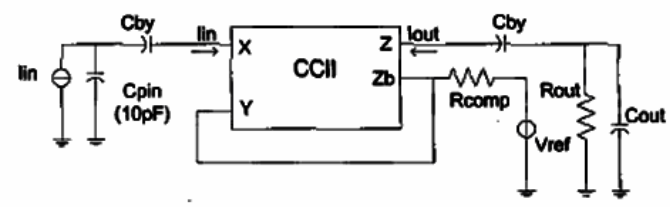

Fig. 2 Second generation current conveyor CCII amplifier [8].

Z_b is a dummy output with characteristics identical to the Z output. The conveyor terminals Y and Z_b have been connected to R_{comp}, grounded to a fixed potential. This feedback scheme promotes a decrease in the input impedance viewed at terminal X. The use of Eq. (1) in this scheme yields the effective input impedance at terminal X as [8]:

$$r_{xcomp} = r_x - \frac{A_v A_i R_{comp}}{1+(g_y + g_i)R_{comp}} \qquad (2)$$

Equation (2) shows that it is possible with this feedback scheme to reduce the effective input impedance to arbitrarily small values. Considering voltage and current gains near unity, a value of R_{comp} near r_x, makes possible to synthesize a zero input impedance. However, the non-ideal high frequency behavior of the conveyor makes these matrix parameters frequency-dependent [7-9].

C. *Basic Cell and Effective Input Dynamic Range*

The basic CCII cell that is used to form the amplifier described in Fig. 2 is shown in Fig. 3.

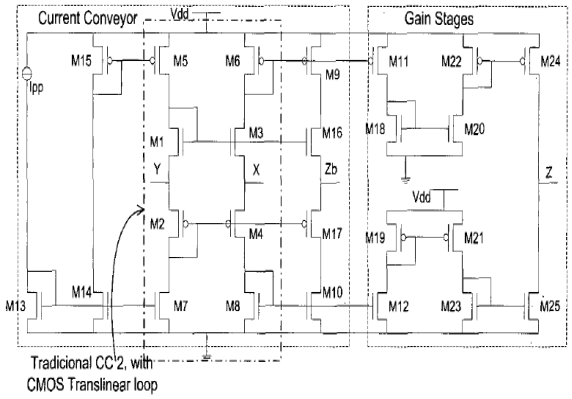

Fig. 3 Second generation current conveyor CCII amplifier basic cell [8].

The linear input range is determined by the operation of the translinear loop [M1 to M4]. So, writing the loop equations reveals that [8]:

$$I_{D4} = I_{D3} + I_x$$
$$V_{gs1} + |V_{gs2}| = V_{gs3} + |V_{gs4}| \qquad (3)$$

Considering that all transistors operate under the saturation condition, Eq. (3) can be resolved for currents I_{D3} and I_{D4}, resulting in:

$$I_{D3,4} = KI_{pp}\left(1 \mp \frac{I_x}{4KI_{pp}}\right) \qquad (4)$$

where I_{pp} is the polarization current, I_x is the input current at node X and k is an aspect ratio between the dimensions of transistors (M1, M2) and (M3 ,M4). This result is valid only for values of I_x between - $4kI_{pp}$ and $4kI_{pp}$. These are the maximum values of the input current (as a first approximation), where the amplifier maintains a linear gain dependence on the input current [8], [9].

III. SIMULATION RESULTS AND DISCUSSION

A. *Effect of Photodiode Internal Capacitance*

In the amplifier of Figs. 2 and 3, one chooses V_{dd}= 12 V, I_{in}= 250 mA, R_{out}= 0.05 kΩ, C_{by}= zero (omitting pad interconnection), R_{comp}= 0.1 kΩ, C_{out} = 10 pF, I_{PP} = 2 mA. W/L for all N-MOS is chosen to be 20 μm/1.2 μm except for M1 and M3 that were designed with a ratio of 70 μm/l.2 μm. W/L for all P-MOS is chosen to be 28 μm/1.2 μm except for M24 which is chosen 1000 μm/0.5 μm. Transistors M12, M20 and M25 have also a different design ratio (40 μm/l.2 μm), in order to provide some gain between the input X and the output Z. Temperature of simulation was set at 27 ^oC.

Values of I_{in} and I_{PP} are chosen to fall in the theoretical limits of linear dynamic range operation as indicated in previous theoretical discussion. Other values are chosen to be near real life values in such systems and are extracted from the published literatures [2], [8] noting that, this choice gives the ability for comparison. Also, as will be seen, it will be proved the advantage of this choice during simulation results. W/L values are optimized as much as possible to give maximum output current gain [9-11].

The influence of photodiode internal capacitance (C_{pin}) on the system bandwidth is discussed in the range of 1 to 50 pF, in which more than 90% of today's practical silicon photodiodes are fabricated and used in WOC systems. Simulation results fairly agree with that published on the effect on the bandwidth, where increasing photodiode capacitance decreases dramatically the bandwidth [2], [3]. Results of simulation are listed in Table 1.

C_{pin} pF	1	10	30	40	50
BW MHz	120.32	30.65	10.21	8.12	7.02

Table 1 Simulation results for CCII amplifier bandwidth, BW, with C_{pin}.

The reason can be extracted from [3], [4] that indicates that increasing the photodiode capacitance results in increasing photodiode effective area which enables photodiode to collect as much radiant optical power as possible. However, this will result in decreasing the operating bandwidth and increasing collected sources of noise. Simulation for C_{pin}=1 pF is shown in

Fig. 4 while other values give the same behavior but with different bandwidths as listed in Table 1.

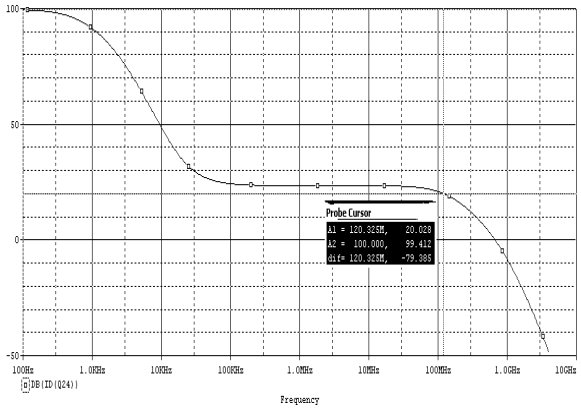

Fig. 4 Simulation of CCII amplifier bandwidth at C_{pin}=1 pF.

Now, we are going to add the effect of changing the same values of photodiode capacitance on the input impedance (R_{in}) noting that all simulation include a value of R_{comp}= 0.1 kΩ and is taken at the corresponding maximum bandwidth obtained in Table 1 (i.e: for C_{pin}=10 pF and the value of R_{in} is extracted at 30.65 MHz). Results obtained are given in Table 2.

C_{pin} pF	1	10	30	40	50
R_{in} Ω	567.72	403.27	400.94	391.51	372.00

Table 2 Simulation results for CCII amplifier input impedance, R_{in} at different values of C_{pin}.

Again, result with C_{pin}=1 pF only is displayed in Fig. 5 while others take the same behavior but with values listed in Table 2.

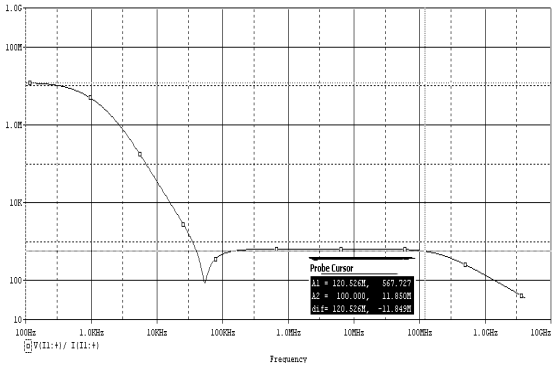

Fig. 5 Simulation of CCII amplifier input impedance at C_{pin}=1 pF.

As indicated, one can observe that, in the range from 50 to 100 MHz, the input impedance decreases with the photodiode capacitance. This range is the interest range since today's available line-of-sight wireless optical technology is looking forward to reach this value (100 MHz), especially in IrDA standards [1], [3] and [4]. One can say that increasing photodiode capacitance can store more of the input current resulting in a decrease in the input impedance.

Now, and after the effect of the photodiode capacitance on the level of input impedance, one can say that a compromise should be done to choose a photodiode with a specific internal capacitance since increasing internal capacitance decreases both the operating bandwidth and the input impedance. However, the change in the operating bandwidth is more noticeable than that of the input impedance level.

This is the main reason for choosing 1 pF as a standard value in the following simulations since a linear bandwidth up to 120.32 MHz is required with small input impedance (567.72Ω). However, this very low value of internal capacitance can cause coupling problems. So, a big care should be taken when positioning the receiver in the line-of-sight of the transmitter. Another solution is to use a large internal capacitance but the price of bandwidth will be paid.

From simulation, it is observed that changing photodiode internal capacitance does not change the high output current level (I_{out}) of M24 (above 19 dB in all cases) and still obtaining high gain (above 38.5 dB in all cases) at a wide range of operating conditions

B. Gain of CCII Amplifier and Power Dissipation

This amplifier under the simulation conditions of Sec. III-A with C_{pin}=1 pF for the reasons discussed achieves the highest gain simulated through all designs that use the same cell and technique [7-9]. The output current (I_{out}) of M24, Fig. 4, is 20.02 dB at 120.32 MHz. This will guide to a current gain (I_{out}/I_{in}) = 40.12. This is shown in Fig. 6.

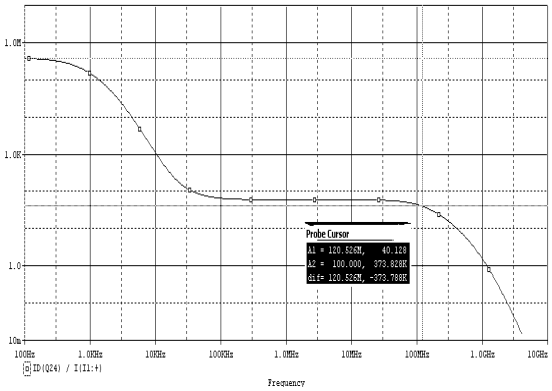

Fig. 6 Simulation of CCII amplifier gain at C_{pin}=1 pF.

However, this large gain is achieved with a price reflected on the large input impedance compared to the same design that uses the same cell and technique [7-9]. So, the application specifications will specify the best suitable design to use. Power dissipation is simulated to be 0.21 W.

C. Verifying Importance of Feedback Control Resistance and its Effects on Bandwidth and Input Impedance.

Simulation of CCII amplifier in Figs. 2 and 3 under the values mentioned in the beginning of Sec. III-A with C_{pin} = 1 pF but without R_{comp} is shown in Figs. 7 and 8.

As one can observe from Fig. 7, omitting feedback control resistance will decrease the allowable bandwidth by ~ 32 MHz (From 120.32 MHz with R_{comp}, Fig.4, to 88.29 MHz without R_{comp}, Fig.7) while maintaining all other simulation parameters unchanged compared with previous section while the level of the output current increase by 2.4 dB. From Fig. 8, the effect of

neglecting R_{comp} reflects on the large value of the input impedance observed (~ 943.65 Ω at 88.29 MHz). This value is about 1.6 times larger than that observed at exactly the same operating point and conditions mentioned in Sec.III-A except the existence of R_{comp}.

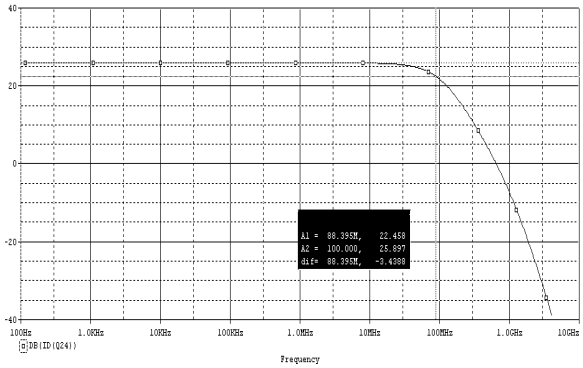

Fig. 7 Simulation of CCII amplifier bandwidth without R_{comp}

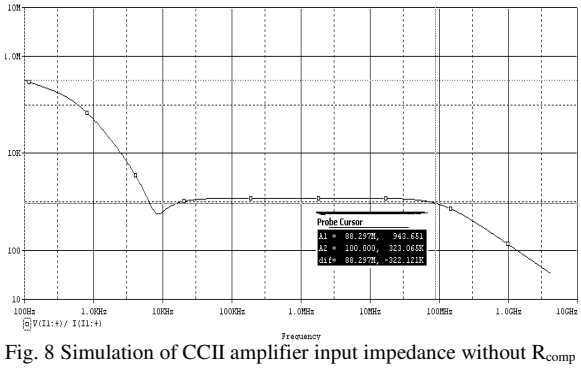

Fig. 8 Simulation of CCII amplifier input impedance without R_{comp}

The following simulation is carried out under the values mentioned in Sec. III-A with C_{pin} = 1 pF but with variable values for R_{comp}. Results of simulation are listed in Table 3.

R_{comp} kΩ	0.1	0.3	0.5	1	1.5
BW MHz	120.32	115.62	110.92	110.00	108.65

Table 3 Simulation results for CCII amplifier bandwidth under different values of R_{comp}

Only the behavior under R_{comp}= 0.3 kΩ is presented in Fig. 9, while other values of the control resistance show the same behavior but with bandwidths listed above.

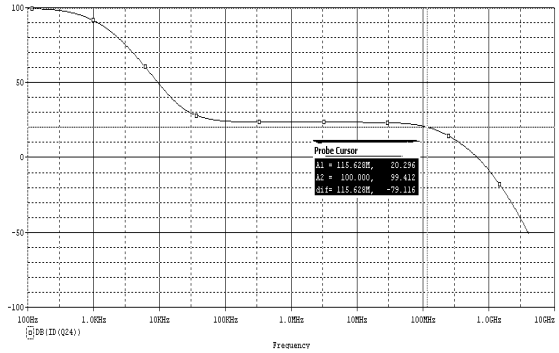

Fig. 9 Simulation of CCII amplifier bandwidth with R_{comp}=0.3 kΩ.

Increasing the control resistance decreases the allowable amplifier linear bandwidth. The reason is mentioned in Ref. [12] where, increasing resistance increases both thermal and shot noise and hence decreases the allowable bandwidth.

The effect of the control resistance (R_{comp}) on the level of input impedance under parameters of Sec. III-A with C_{pin} = 1 pF and at the corresponding bandwidth obtained in Table 3 (i.e: for R_{comp}= 0.3 kΩ value of R_{in} was extracted at 115.62 MHz) is tabulated in Table 4.

R_{comp} kΩ	0.1	0.3	0.5	1	1.5
R_{in} Ω	567.72	575.94	582.22	587.23	592.89

Table 4 Simulation results for CCII amplifier input impedance under different values of R_{comp}

The behavior under R_{comp}= 0.3 kΩ is displayed in Fig. 10. Again, other values of the control resistance show the same behavior with amplitudes listed above.

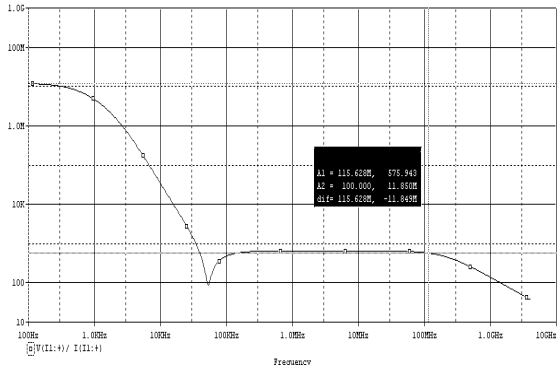

Fig. 10 Simulation of CCII amplifier input impedance with R_{comp} = 0.3 kΩ.

One can observe that, the increase in control feedback resistance will increase the level of input impedance with a very small amount. This is an advantage of the amplifier since approximately constant behavior under a wide operating rage is achievable.

As a conclusion for this point, the amplifier achieves both wide bandwidth with low input impedance in a very wide range of control resistance. So, any abrupt change in its value due to surrounding environment or sudden noise will not dramatically affect its performance. However, omitting the control resistance from the design will degrade the behavior of the amplifier. From this point, one can understand the good choice of R_{comp}= 0.1 kΩ in all simulations starting from Sec. III-A since the value of input impedance is relatively low and the bandwidth is the largest. Also, changing the control resistance does not change the high output current level (above 19.5 dB in all cases) and still obtaining high gain (above 39 dB in all cases) at a wide range of operating conditions

D. Effect of Temperature

Simulation conditions and values will be set as mentioned in the beginning of Sec. III-A with C_{pin} = 1 pF and R_{comp}= 0.1 kΩ for the reasons discussed but at different operating temperatures. Results of simulation are listed in Table 5.

T °C	5	15	27	40	50
BW MHz	127.98	122.82	120.32	117.87	108.65

Table 5 Simulation results for CCII amplifier bandwidth at different operating temperatures.

The behavior at T = 50 °C is presented in Fig 11. The other studied temperatures give the same behavior but with different bandwidths, Table 5.

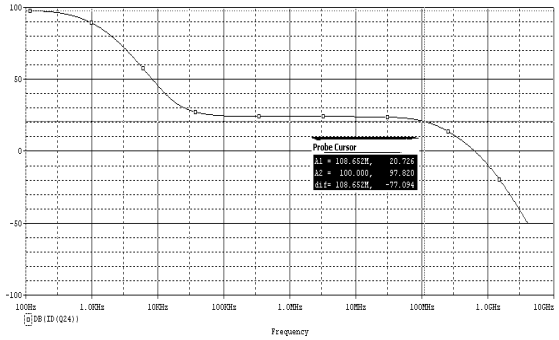

Fig. 11 Simulation of CCII amplifier bandwidth with T=50 °C.

As expected, increasing temperature decreases the allowable bandwidth of the CCII buffer. This is explained as follows: increasing temperature will increase the thermal noise generated in the circuit and hence limits the operating bandwidth. Simulation shows a fair agreement with the theoretical background discussed in details as in [3], [4].

Now, we are going to investigate the effect of temperature on the input impedance (R_{in}) under same conditions at the beginning of this section and at the corresponding bandwidth obtained in Table 5 (i.e: for T= 50 °C and the value of R_{in} is extracted at 108.65 MHz). Results of simulation are listed in Table 6.

T °C	5	15	27	40	50
R_{in} Ω	512.15	539.30	567.72	597.19	629.19

Table 6 Simulation results for CCII amplifier input impedance under different values of temperature.

Again, the results obtained at 50 °C are presented in Fig. 12, while other temperatures give the same behavior with the values of R_{in} found in Table 6.

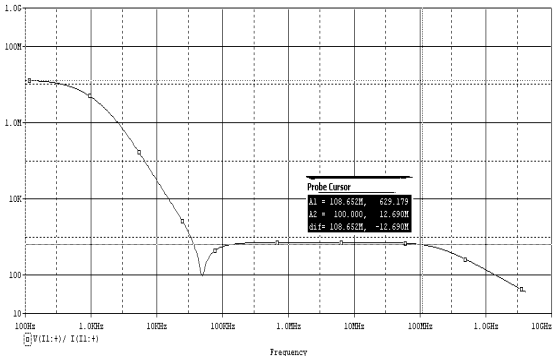

Fig. 12 Simulation of CCII amplifier input impedance with T= 50 °C.

As indicated from the simulation, increasing the operating temperature increases the input impedance level. The reason for that may be what is mentioned on the relation between bandwidth and temperature and discussed early in this section. However, within all temperature variations, the amplifier maintains its high output current level (above 19.3 dB in all cases) and still obtaining high gain (above 38 dB in all cases).

E. Effect of Load Resistance

The simulation conditions are set as mentioned in Sec. III-A, with C_{pin} = 1 pF and R_{comp}= 0.1 kΩ and the effect of the load resistance (R_{out}) is shown in Table 7.

R_{out} Ω	50	100	150	200	250
BW MHz	120.32	205.35	279.53	336.34	430.45
I_{out} db	20.02	-3.31	-11.37	-16.09	-20.45

Table 7 Simulation results for CCII amplifier bandwidth under different values of R_{out}.

Figure 13 displays the obtained results for a load resistance R_{out}=100 Ω and other results shows same behavior with values listed in Table 7, except at a high resistive load as explained later.

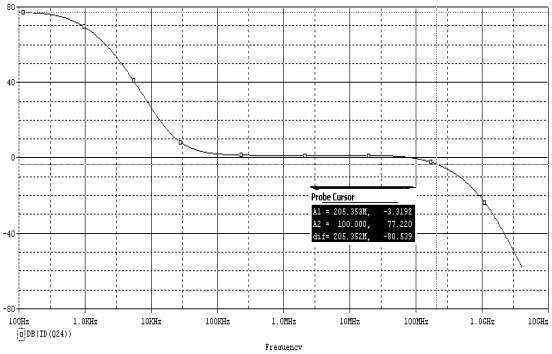

Fig.13 Simulation of CCII amplifier bandwidth with R_{out}=100 Ω.

For the first time, in Table 7, we include the value of the output current (I_{out}) of M24. This is because in all previous studied parameters and under a wide range of variable conditions, I_{out} maintains approximately above 19.5 dB leading to a gain above 38 dB. These values, as previously indicated, are the highest compared with similar designs using same technique and cell [7-9]. However, by varying the resistive load (R_{out}), this advantage is no longer available. From Table 7, one observes that, increasing the resistive load R_{out}, a linear operating bandwidth is improved significantly while the level of the output current and hence the gain decreases dramatically. Also, at an extreme resistive load (50 kΩ), ripples are noticed in the spectrum leading to a distorted behavior. This shows a fair agreement with that published in Ref. [8]. These simulations lead to a conclusion that it is important to operate this amplifier under low resistive load to get the advantage of both high gain and bandwidth or use extra circuits and hence extra noise to deal with high resistive loads.

Now, under the same simulation values and parameters mentioned, we are going to perform a simulation for the effect of load resistance on the input impedance at the corresponding bandwidth obtained in Table 7 (i.e: for R_{out}= 100 Ω and at R_{in}

extracted at ~ 205.35 MHz). Results of simulation are listed in Table 8.

R_{out} Ω	50	100	150	200	250
R_{in} Ω	567.72	464.70	389.31	343.44	288.55

Table 8 Simulation results for CCII amplifier input impedance under different values of R_{out}.

The input impedance is displayed in Fig. 14 at R_{out}= 100 Ω. Other values of R_{out} give the same behavior but with input impedance found in Table 8.

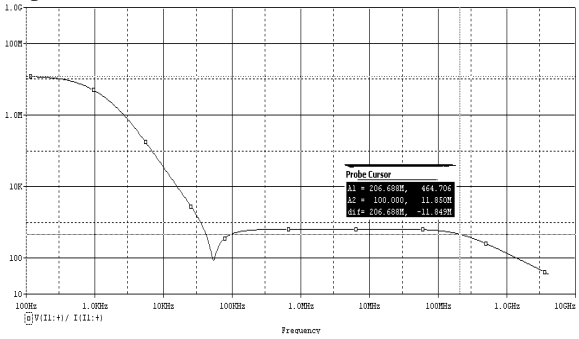

Fig. 14 Simulation of CCII amplifier input impedance with R_{out}=100 Ω**.**

It is clear that increasing resistive load will decrease the input impedance which may be considered as an advantage. It is easily concluded that increasing R_{out} will enhance both the linear operating bandwidth with the input impedance. The big cost is paid for that enhancement on the level of output current and hence the gain. So, one can understand the good choice of R_{out}= 50 Ω through all of simulations starting from Sec III-A since simulation at this value provides high gain together with high bandwidth (with respect to today's IrDA applications) and a reasonable value of the input impedance.

F. Effect of Load Capacitance

Similar to previous effects, the simulation conditions are set as mentioned in Sec. III-A, with C_{pin} = 1 pF and R_{comp}= 0.1 kΩ. The effect of variable load capacitance C_{out} is simulated in Table 9.

C_{out} pF	10	30	50	70	100	150
BW MHz	120.3	153.9	181.52	170.66	160.45	150.85

Table 9 Simulation results for CCII amplifier bandwidth under different values of C_{out}.

Figure 15 displays the obtained results for load capacitance at C_{out}= 150 pF and other values show same behavior with values listed in Table 9.

As indicated from simulation results, the capacitive load increases the linear operating bandwidth until reaching the near C_{out}= 50 pF. After that, the behavior is inverted. Simulation at high capacitive load C_{out}= 700 pF indicates that bandwidth decreases to reach 133.5 MHz without distorted behavior as in resistive load. The output current level and hence the gain, in all cases of Table 9, are over 20 dB and 40 dB, respectively.

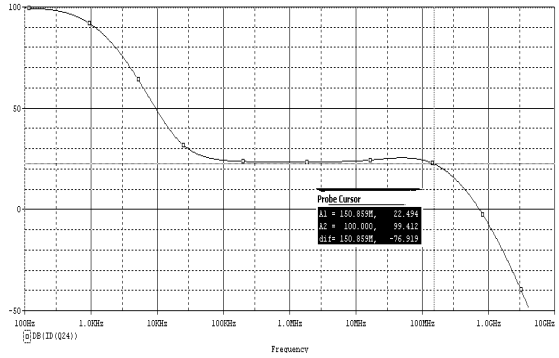

Fig. 15 Simulation of CCII amplifier bandwidth with C_{out}= 150 pF.

Now, under the same simulation values and parameters mentioned, we are going to carry a simulation for effect of load capacitance on the input impedance at the corresponding bandwidth obtained in Table 9 (i.e: for C_{out}= 150 pF and at R_{in} extracted at ~ 150.85 MHz). Results of simulation are listed in Table 10.

C_{out} pF	10	30	50	70	100	150
R_{in} Ω	567.7	525.98	493.11	507.56	518.02	529.94

Table 10 Simulation results for CCII amplifier input impedance under different values of C_{out}.

The input impedance is displayed in Fig. 16 at C_{out}=150 pF, while other values of the load capacitance have the same behavior but with the input impedance found in Table 10.

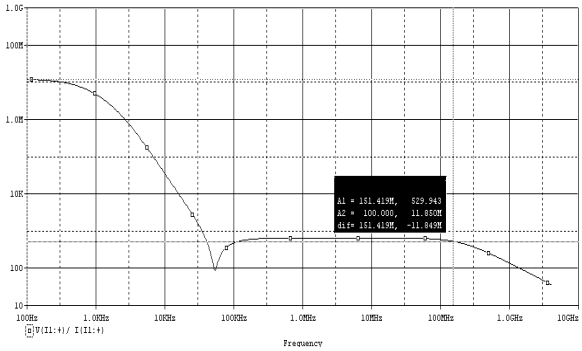

Fig. 16 Simulation of CCII amplifier input impedance with C_{out}=150 pF**.**

From the obtained results, the amplifier can operate at a wide range of the capacitive load without drawbacks on its high gain and high bandwidth. Also, a reasonable value of the input impedance is achieved through all simulation conditions.

G. Equivalent Input Current Noise (EICN) and Effect of Photodiode Internal Capacitance

The effect of the photodiode internal capacitance on the level of the equivalent input current noise level is studied. Simulation conditions and values are set as mentioned in Sec. III-A with C_{pin} = 1 pF. The input noise is defined as the equivalent noise that would be needed at the input source to generate the calculated output noise in an ideal (noiseless)

circuit [12]. The input current noise level was simulated at the photodiode internal capacitance values and their corresponding bandwidth presented in Table 1 to give a global indication about the effect of C_{pin} (i.e: for C_{pin}= 1 pF and the value of EICN was extracted at ~ 120.32 MHz). Results of simulation are shown in Table 11.

C_{pin} pF	1	10	30	40	50
EICN pA/(Hz)$^{0.5}$	14.59	35.25	133.53	196.41	261.81

Table 11 Simulation results for CCII amplifier EICN, under different values of C_{pin}.

Only the behavior at C_{pin} =1 pF is presented in Fig. 17, while other values of the photodiode capacitance have the same EICN behavior with the values in Table 11.

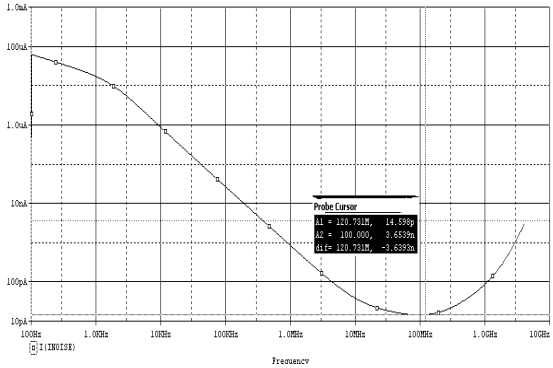

Fig. 17 Equivalent input current noise level for CCII amplifier at C_{pin}=1 pF.

As expected, the equivalent input noise current increases with the photodiode capacitance since it widens the photodiode effective area and collects more radiant power including noise. This observation shows a fair agreement with [3], [4]. From the simulations, increasing photodiode internal capacitance decreases the allowable bandwidth and increase the EICN which is a drawback. On the other hand, this increase lowers the value of the input impedance and makes the positioning between transmitter and receiver more easily leading to minimize coupling and receiving problems. The present CCII amplifier EICN (especially when C_{pin}=1 pF) shows a very low EICN compared with [8] which uses the same technique and cell at 120.32 MHz.

H. Output Noise Level

This level defines the RMS sum of all the device contributions propagated to a specified output net [12]. Output net in the amplifier is that attached to the load resistance or capacitance. Many sources of noise through the devices were simulated. For example, diodes have separate noise contributions from thermal, shot, and flicker noise [12]. This is done for all parts of circuit. Simulation conditions and values are set as mentioned in Sec. III-A with C_{pin} = 1 pF. The value of the output simulated noise level was extracted at 120.32 MHz since it is the corresponding bandwidth obtained in Table 1.

The amplifier shows a very small output voltage noise level. This value, as indicated from Fig. 18, is 27.40 nV/(Hz)$^{0.5}$ and indicates that small amount of noise will be transferred in the following attaching circuits. However, as mentioned before, the price is paid in the relatively large value of the input impedance. So, a compromise should be done.

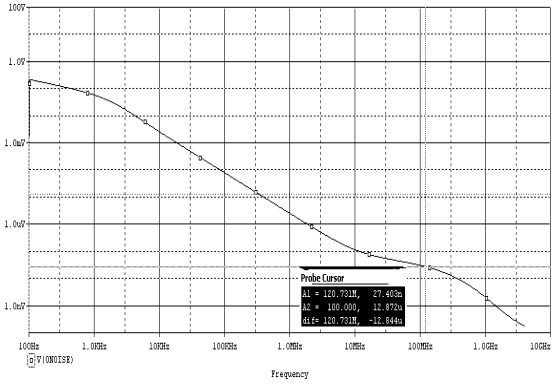

Fig. 18 Output noise level for CCII amplifier.

IV. CONCLUSION

This work is very important to answer a part of the problems of the WOC outdoor applications. We believe that the use of the described amplifier attached to a transimpedence amplifier can enhance the receiving characteristics of any outdoor WOC receiver making it possible to get the advantage of a part of the huge optical domain properties. This work can help designers of outdoor practical optical receivers to handle signals with a huge knowledge about variable affecting parameters and how to deal with.

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