A Current-Conveyor Based Buffer for High-Bandwidth and Low Input-Impedance Outdoor WOC Applications

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Abstract— **This work presents a method for solving an outdoor WOC receiving problem. A current conveyor based buffer is designed and simulated under wide range of operating conditions. Effects on bandwidth and input impedance are simulated and compared with previously designed architectures resulting in a better performance. Parameters that affect the design are investigated including photodiode internal capacitance, control feedback resistance, resistive and capacitive loads, temperature, input and output noise levels. OrCAD 10.5 used as a simulation tool in the paper.**

Index Terms—**ClassII current conveyor, Control feedback technique, Equivalent input current noise level, Photodiode internal capacitance, Wireless optical communication.**

I. INTRODUCTION

Infrared free-space optical receivers find applications in laptop computers, cellular phones, digital cameras, computer peripherals, personal digital assistants, and many other consumer electronics equipped with a short-distance infrared communication port. In infrared wireless optical receivers, the use of sensitive current-input preamplifiers or buffer to process the signal currents from photodiodes is essential. Infrared wireless preamplifiers or buffer require a wide bandwidth, a wide dynamic range, and the ability to reject ambient light. According to Infrared Data Association (IrDA), data rates of 100Mb/s and higher are now being investigated [1], [2].

An example of those are high-speed optical air links developed, using low cost photodiodes attached to CMOS-based transimpedance front-ends in [3], [4]. This system is an example of an outdoor wireless optical communication (WOC) problem: these are situations when low current, high bandwidths signals should be able to go through large capacitance nodes, but the capacitive load in these nodes severely restricts overall system bandwidth [5], [6].

A novel current-conveyor based buffer, able to handle differential signals, was introduced in [7] and used effectively as a technique in [7-9] to solve this problem. This buffer uses class-II Current Conveyor concepts (CCII) to implement a controlled low input impedance system. Using this buffer to interconnect a photodiode with a state-of-the-art transimpedance amplifier has increased significantly the performance of the system.

In this paper, we are going to use the basic CCII buffer introduced with modifications to solve the previously discussed problem. The paper contribution includes discussing the effects of: existence of feedback technique, temperature, practical margins of load resistance and capacitance, internal photodiode capacitance on equivalent input current noise level. Finally, it introduces the concept of output noise level with simulations.

The paper is organized as follows: Section II introduces the mathematical and theoretical information about CCII based cell in: modeling scheme, input impedance control and effective input dynamic range. The theoretical background with the used diagram for CCII buffer followed by simulation and discussion are found in Sec. III and the conclusion is introduced in Sec. IV.

II. THEORETICAL AND MATHMATICAL BACKGROUND

A. *Modeling of CCII*

A second generation current conveyor block diagram CCII is shown in Fig. 1.

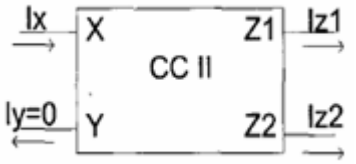

Fig. 1 Second generation current conveyor basic cell [8].

This diagram can be adequately described by the following matrix equation [8]:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{pmatrix} g_y & 0 & 0 \\ A_v & r_x & 0 \\ 0 & A_i & g_z \end{pmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

The elements inside the system matrix represent the relevant parameters of the current conveyor which are frequency dependent. A_V represents the voltage gain between the input nodes X and Y and A_i represents the current gain between the X input and one generic Z output. V_x , V_y *and* V_z are, respectively, voltages at points x, y and z. I_x , I_y *and* I_z are the corresponding currents and r_x is the effective input impedance. In order to include both the effects of the inputs (X and Y) and the output (Z), the system matrix takes into account the impedances (admittances) at ports X, Y and Z. High frequency effect should be taken in consideration through all procedures [8].

B. Input Impedance Control

CCII input impedance can be controlled by the circuit depicted in Fig. 2. This figure includes the basic CCII cell attached to circuits that can specify its operation. Attached circuits include a model for the input photodiode (**I_{in}** and C_{pin} are the photocurrent and photodiode capacitance), pad interconnections (C_{by} is a bypass capacitor), control resistance R_{comp}, and buffer load (R_{out} and C_{out}) [7], [8].

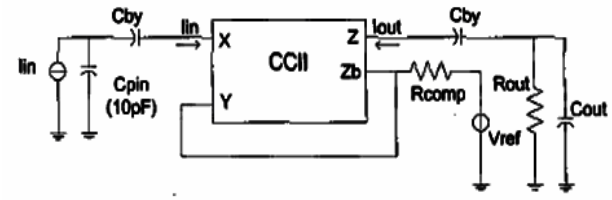

Fig. 2 Second generation current conveyor CCII buffer [8].

Z_b is a dummy output with characteristics identical to the Z output. The conveyor terminals Y and Z_b have been connected to a feedback control resistance (R_{comp}), grounded to a fixed potential. This feedback scheme promotes a decrease in the input impedance viewed at terminal X**.** When this scheme is using equation (1), the effective input impedance at terminal X is given by [8]:

$$r_{xcomp} = r_x - \frac{A_v A_i R_{comp}}{1 + (g_y + g_i) R_{comp}} \quad (2)$$

Equation 2 shows that it is possible with this feedback scheme to reduce the effective input impedance to arbitrarily small values. Considering voltage and current gains near unity, a value of R_{comp} near r_x, makes possible to synthesize a zero input impedance. However the non-ideal high frequency behavior of the conveyor makes these matrix parameters frequency-dependent [7-9].

C. Basic Cell and Effective Input Dynamic Range

The basic CCII cell that can be used to form a buffer or amplifier and will be used to form our buffer described in Fig. 2 is shown in Fig. 3.

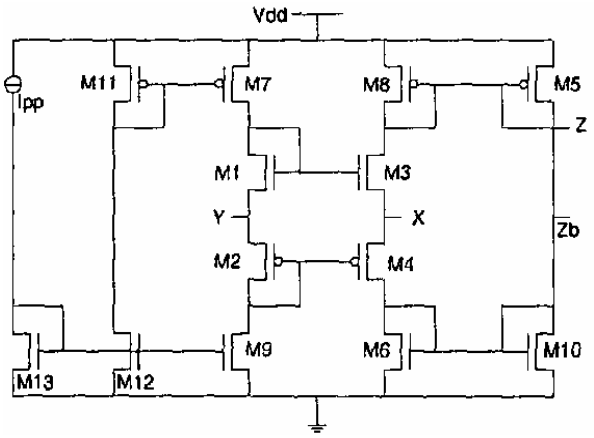

Fig. 3 Second generation current conveyor CCII basic cell [7].

The linear input range is determined by the operation of the translinear loop [M1 to M4]. So writing the loop equations reveals that [8]:

$$\begin{aligned} I_{D4} &= I_{D3} + I_x \\ V_{gs1} + |V_{gs2}| &= V_{gs3} + |V_{gs4}| \end{aligned} \quad (3)$$

Considering that all transistors operate under the saturation condition, equation (3) can be resolved for currents I_{D3} and I_{D4}**,** resulting in:

$$I_{D3,4} = KI_{pp}\left(1 \mp \frac{I_x}{4KI_{pp}}\right) \quad (4)$$

where I_{pp} is the polarization current, I_x is the input current at node X and *k* is an aspect ratio between the dimensions of transistors (M1, M2) and (M3 ,M4). This result is valid only for values of I_x between $-4kI_{pp}$ and $4kI_{pp}$: these are the maximum values of the input current (as a first approximation) where the amplifier or buffer maintains a linear gain dependence on the input current [8], [9].

III. SIMULATION RESULTS AND DISCUSSION

A. *Effect of Photodiode Internal Capacitance, Gain of Buffer and Power dissipation.*

In buffer of Figs. 2 and 3, one chooses V_{dd}= 2 volt, I_{in}= 130 mA, R_{out}= 0.05 kΩ, C_{by}= zero (omitting pad interconnection), R_{comp}= 0.1 kΩ, C_{out}=10 pF, I_{PP}= 2 mA. W/L for all N-MOS is chosen to be 50 µm /1.2 µm. W/L for all P-MOS is chosen to be 125µm/1.2 µm except for M5, Fig. 3, which is chosen 1000 µm /0.5 µm. Temperature of simulation was set at 27 ^{o}C.

Values of I_{in} and I_{PP} are chosen to fall in the theoretical limits of linear dynamic range operation as indicated in previous theoretical discussion. Other values are chosen to be near real life values in such systems and are extracted from the published literatures [2], [7] and [8] noting that, this choice gives the ability for comparison. Also, as will be seen, it will be proved the advantage of this choice during simulation results. W/L values are optimized as much as possible to give maximum current gain without using any additional circuits or current mirror structures [10], [11].

The influence of photodiode capacitance, C_{pin}, on the system bandwidth is discussed in the range of 1 to 50 pF in which more that 90% of today's practical Si photodiodes are fabricated and used in WOC systems. Simulation results agree with that published on the effect on the bandwidth where increasing photodiode capacitance decreases dramatically the bandwidth [2], [3]. Results of simulation are listed in Table 1.

C_{pin} pF	1	10	30	40	50
BW MHz	210.378	189.671	126.183	108.143	92.683

Table. 1 Simulation results for CCII buffer bandwidth, BW, with C_{pin}.

The reason can be extracted from [3], [4] that indicated increasing photodiode capacitance results in increasing photodiode effective area which enables photodiode to collect as much radiant optical power as possible. However, this will result in decreasing operating bandwidth and increasing collected sources of noise. Simulation for C_{pin}=1 pF is shown in Fig. 4 while other values take the same behavior but with different bandwidth values as listed in Table 1.

Now, we are going to add the effect of changing the same values of photodiode capacitance on the input impedance (R_{in}) noting that all simulation include a value of R_{comp}= 0.1 kΩ and is taken at 190 MHz. Results obtained are given in Table 2.

C_{pin} pF	1	10	30	40	50
R_{in} Ω	27.21	25.69	19.19	16.33	14.05

Table. 2 Simulation results for CCII buffer input impedance, R_{in} at different values of C_{pin}.

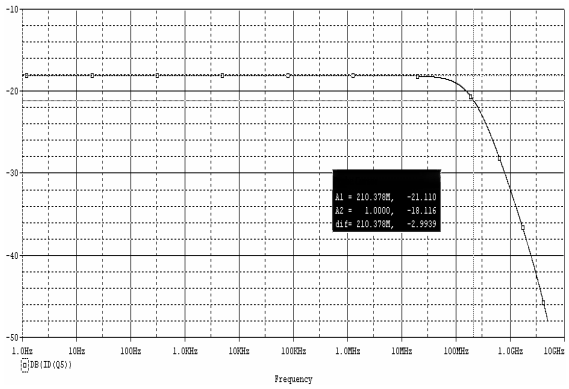

Fig. 4 Simulation of CCII buffer bandwidth at C_{pin}=1 pF.

The reason can be extracted from [3], [4] that indicated increasing photodiode capacitance results in increasing photodiode effective area which enables photodiode to collect as much radiant optical power as possible. However, this will result in decreasing operating bandwidth and increasing collected sources of noise. Simulation for C_{pin}=1 pF is shown in Fig. 4 while other values take the same behavior but with different bandwidth values as listed in Table 1.

Again, result with C_{pin}=1 pF only is displayed in Fig. 5 while others take the same behavior but with values listed in Table 2.

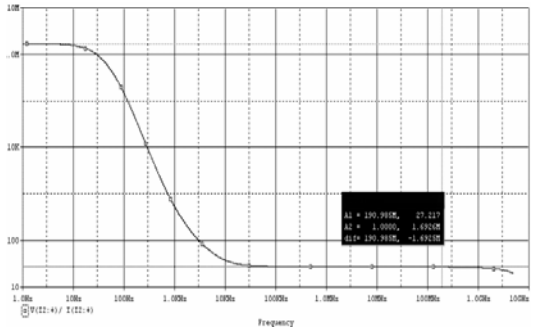

Fig. 5 Simulation of CCII buffer input impedance at C_{pin}=1 pF.

As indicated, one can observe that in the range from 50 to 100 MHz input impedance will decrease as the photodiode capacitance increased. This range is the interest range since today's available line-of-sight wireless optical technology looking forward to reach this value (100 MHz), especially IrDA standards [1], [3] and [4]. One can say that increasing photodiode capacitance can store more of the input current resulting in a decrease in the input impedance.

Now, and after adding the effect of changing photodiode capacitance on the level of input impedance, one can say that a compromise should be done to choose a photodiode with specific internal capacitance since increasing internal capacitance decreases both the operating bandwidth and the input impedance. However, the change in the operating bandwidth is more noticeable than in that of the input impedance level. This is the main reason for choosing 10 pF as standard value in the following simulations since a linear bandwidth up to 189.671 MHz with relatively small input impedance (25.69 Ω) is obtained without no coupling problems results from very low internal capacitance values of photodiodes and avoiding collecting much noise at large photodiode capacitance.

Unfortunately, the buffer does not achieve the unity gain operation under the simulation bandwidth. Maximum obtained gain (I_{out}/I_{in}) with is 0.961. We think this problem is due to the simplicity of our design and not using extra circuitry or current amplification techniques attached to CCII cell to increase the gain as in [7], [8]. Noting that additional circuitry will add more noise and cost and lowers the operating bandwidth of the buffer. Though, the buffer is still interesting with its very high bandwidth and extremely low input impedance, low input current noise level and low output noise level as will be proved in the following sections. Total Power dissipation under the previously mentioned conditions is 68 mW which is little higher in comparison with literatures using same cell and technique [8].

B. Verifying Importance of Feedback Control Resistance and its Effects on Bandwidth and Input impedance.

Simulation of CCII buffer in Fig. 2 and 3 under the values mentioned in the beginning of Sec. III-A with C_{pin} = 10 pF but without R_{comp} is shown in Figs. 6 and 7.

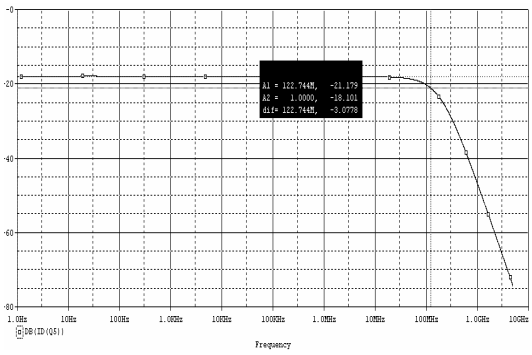

Fig. 6 Simulation of CCII buffer bandwidth without R_{comp}

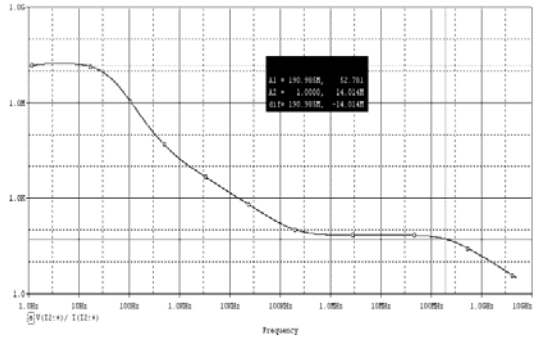

Fig. 7 Simulation of CCII buffer input impedance without R_{comp}

As one can observe from Fig. 6, omitting feedback control resistance will decrease allowable bandwidth by 67 MHz compared with previous section. From Fig. 7, the effect of neglecting R_{comp} reflects on the large value of the input impedance observed (~ 52.78 Ω at 190 MHz). This value is about two times larger than that observed at exactly the same operating point and conditions mentioned in Sec.III-A except the existence of R_{comp}.

The following simulation is carried out under values mentioned in Sec. III-A with C_{pin} = 10 pF but with variable values for R_{comp}. Results of simulation are listed in Table 3.

R_{comp} kΩ	0.1	0.3	0.5	1	1.5
BW MHz	189.671	167.1	158.855	154.52	154.4

Table. 3 Simulation results for CCII buffer bandwidth under different values of R_{comp}

Only the behavior under R_{comp}= 0.1 kΩ is presented in Fig 8 while other control resistance values have the same behavior but with bandwidths listed above.

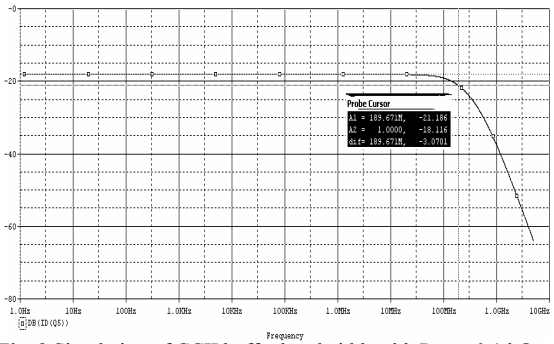

Fig. 8 Simulation of CCII buffer bandwidth with R_{comp}=0.1 kΩ.

Increasing control resistance decreases the allowable buffer linear bandwidth. The reason is mentioned in [12] where, increasing resistance increases both thermal and shot noise and hence decreases the allowable bandwidth. The effect of the control resistance R_{comp} under parameters of

Sec. III-A and at 190MHz on the level of the input impedance (R_{in}) is tabulated in Table 4.

R_{comp} kΩ	0.1	0.3	0.5	1	1.5
R_{in} Ω	25.698	25.695	25.691	25.687	25.686

Table. 4 Simulation results for CCII buffer input impedance under different values of R_{comp}

The behavior under R_{comp}=0.1 kΩ is displayed in Fig 9 while other values of the control resistance have the same behavior with amplitudes listed above. One can observe that, the control feedback resistance has a negligible effect on the value of the input impedance. This is an advantage of our buffer since a constant behavior under a wide operating rage is achievable.

As a conclusion for this point, the buffer achieves simultaneously wide bandwidth with very low input in a very wide range of control resistance. So, any abrupt change in its value due to surrounding environment or sudden noise will not affect its performance dramatically. However, omitting the control resistance from the design will degrade the behavior of the buffer. From this point, one can understand the good choice of R_{comp}= 0.1 kΩ since the value of input impedance is low and the bandwidth is the largest.

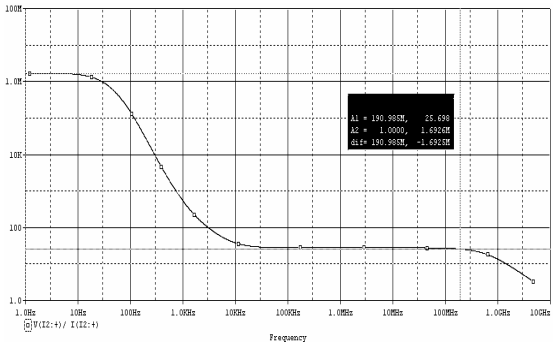

Fig. 9 Simulation of CCII buffer input impedance with R_{comp}=0.1 kΩ.

C. *Effect of Temperature*

Simulation conditions and values will be set as mentioned in the beginning of Sec. III-A with C_{pin} = 10 pF and R_{comp}= 0.1 kΩ but with variable operating temperatures. Results of simulation are listed in Table 5.

T °C	5	15	27	40	50
BW MHz	194.53	190.54	189.67	184.92	180.3

Table. 5 Simulation results for CCII buffer bandwidth under different values of temperature.

The behavior at T = 5 °C is presented in Fig 10. The other studied temperatures gave the same behavior but with different bandwidths, Table 5.

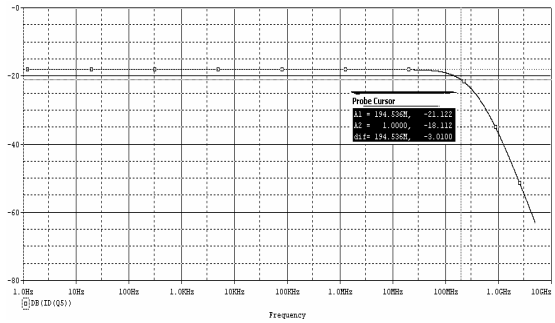

Fig. 10 Simulation of CCII buffer bandwidth with T=5 °C.

As expected, increasing temperature decreases the allowable bandwidth of the CCII buffer. This is explained as follows: increasing temperature will increase the thermal noise generated in the circuit and hence limits the operating bandwidth. Simulation shows a fair agreement with the theoretical background discussed in details as in [3], [4]. Now, we are going to investigate the effect of temperature on input impedance under conditions of Sec. III-A. Results of simulation are listed in Table 6.

T °C	5	15	27	40	50
R_{in} Ω	23.98	24.76	25.69	26.7	27.46

Table. 6 Simulation results for CCII buffer input impedance under different values of temperature.

Again, the results obtained at 5 °C are presented in Fig 11 while other temperatures give the same behavior with the values found in Table 6.

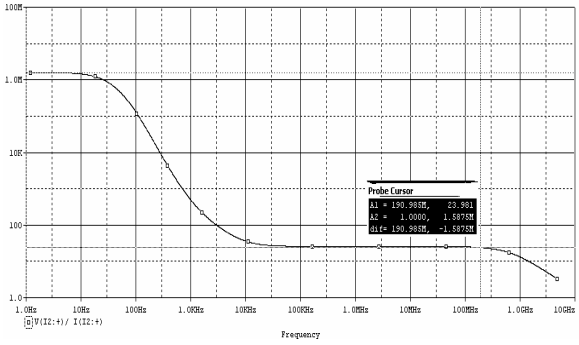

Fig. 11 Simulation of CCII buffer input impedance with T= 5 C.

D. *Effect of Load Resistance*

The simulation conditions are set as mentioned in Sec. III-A, and the effect of R_{out} is listed in Table 7.

R_{out} kΩ	0.05	0.5	5	30	50
BW MHz	189.671	110.918	100.231	97.499	97.499

Table. 7 Simulation results for CCII buffer bandwidth under different values of R_{out}.

Figure 12 displays the obtained results for R_{out}=0.5 kΩ and the results (showing same behavior) for the other values of output resistance are listed in Table 7.

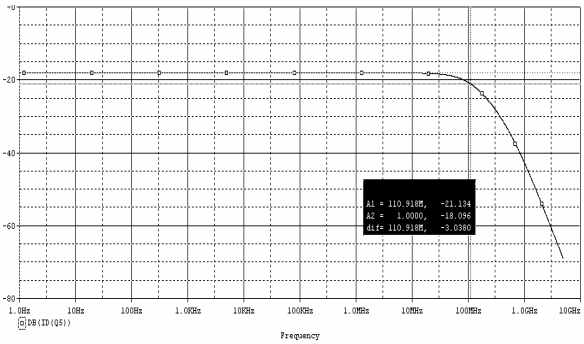

Fig. 12 Simulation of CCII buffer bandwidth with R_{out}=0.5 kΩ.

As observed, the allowable bandwidth decreases with the load resistance. However, the buffer still maintains high bandwidth (97.499 MHz) at extremely high load resistance (50 kΩ). Again, additional noise introduced by additional load resistance may be the reason for the decrease in the bandwidth [12].

Now, under the same simulation values and parameters in Sec. III-A and for the same values of R_{out} we are going to carry a simulation for effect of load resistance on the input impedance. Results of simulation are listed in Table 8.

R_{out} kΩ	0.05	0.5	5	30	50
R_{in} Ω	25.698	25.579	25.532	25.526	25.526

Table. 8 Simulation results for CCII buffer input impedance under different values of R_{out}.

The input impedance is displayed in Fig. 13 at R_{out}=0.5 kΩ, while other values of the load resistances have the same behavior but with input impedance found in Table 8.

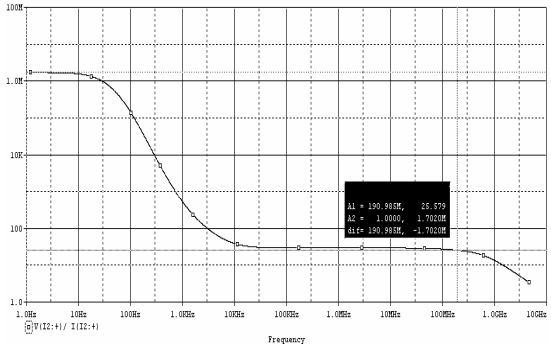

Fig. 13 Simulation of CCII buffer input impedance with R_{out} = 0.5 kΩ**.**

It is clear that, the load resistance has not a significant effect on the input impedance level. This is because the design makes input impedance only strongly dependent on the control feedback resistance which makes this parameter with a constant behavior and hence advances the reliability of the buffer for WOC applications. This result has a fair agreement with that published in Refs. [7], [8].

As a conclusion for the effect of load resistance, the buffer can handle wide variations of these loads and still achieves very low input impedance with a bandwidth near to 100 MHz at extremely high resistive load values. From this point, one can observe the good choice of R_{out}= 0.05 kΩ in all simulation since it achieves the largest bandwidth with the lowest input impedance under the same simulating conditions.

E. Effect of Load Capacitance

The simulation conditions are set as mentioned in Sec. III-A, and the effect of C_{out} is listed in Table 9.

C_{out} pF	10	30	50	70	100
BW MHz	189.67	180.3	175.79	171.39	167.1

Table. 9 Simulation results for CCII buffer bandwidth under different values of C_{out}.

Only the behavior at C_{out} = 30 pF is presented in Fig. 14 as a sample result, where the other capacitance values have same behavior but with bandwidths listed in Table 9.

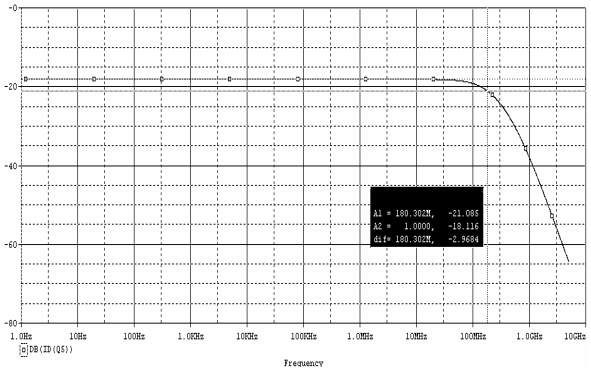

Fig. 14 Simulation of CCII buffer bandwidth with C_{out}=30 pF.

It is clear that increasing load capacitance from 10 to 100 pF results in decreasing the allowable bandwidth. But, the design still achieves very high bandwidth (greater than 100 MHz) more than that required by IrDA at extremely high capacitive loads.

Now, we are going to study the effect of capacitive load on input impedance level under previous conditions and at 190 MHz. The obtained simulation results of are listed in table 10.

C_{out} kΩ	10	30	50	70	100
R_{in} Ω	25.69	25.67	25.65	25.63	25.61

Table. 10 Simulation results for CCII buffer input impedance under different values of C_{out}

Only the behavior at C_{out}= 30 pF is presented in Fig. 15, where the other values show the same behavior but with input impedance values of Table 10.

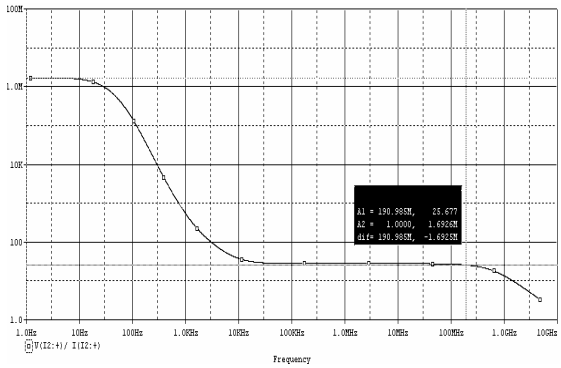

Fig. 15 Simulation of CCII buffer input impedance with C_{out}=30pF.

Here, the increase of the load capacitance does not significantly affect the input impedance level. This is because the design makes the input impedance highly dependent on the control feedback resistance which makes this parameter with a constant behavior and hence improves the reliability of our buffer for WOC applications. This result has fair agreement with the theoretical background in [7], [8]. Now, one can understand why the value of C_{out} is chosen to be 10 pF at Sec. III-A and used in all simulations which provides the highest allowable bandwidth with corresponding low level of input impedance.

F. Equivalent Input Current Noise (EICN) and Effect of Photodiode Internal Capacitance.

The effect of the photodiode internal capacitance on the level of equivalent input current noise level is studied. Simulation conditions and values are set as mentioned in Sec. III-A. The definition of input noise is the equivalent noise that would be needed at the input source to generate the calculated output noise in an ideal (noiseless) circuit [12]. Results of simulation at 100 MHz are listed in Table 11.

C_{pin} pF	1	10	30	40	50
EICN $pA/(Hz)^{0.5}$	104.86	106.31	117.28	126.08	136.56

Table 11 Simulation results for CCII buffer equivalent input current noise level, ENL, under different values of C_{pin}.

Only the behavior at C_{pin} =10 pF is presented in Fig. 16 while other values of the photodiode capacitance have the same behavior with the values in Table 11.

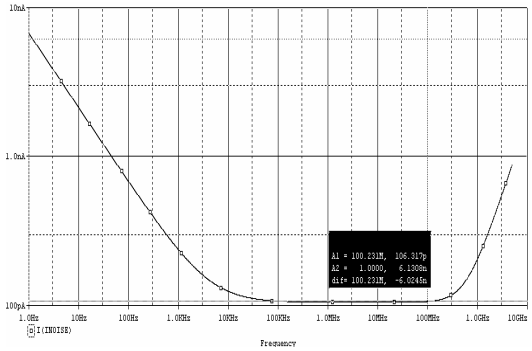

Fig. 16 Equivalent input current noise level for CCII buffer at C_{pin}=10 pF.

As expected, increasing photodiode capacitance increases the equivalent input noise current since it widens the photodiode effective area and collects radiant power including noise. This observation shows a fair agreement with [3], [4]. The present CCII buffer equivalent input current noise level (specially when C_{pin}=10 pF) shows approximately constant behavior in a wide range of bandwidth (100 kHz to 100 MHz) without any oscillations. The value of equivalent input current noise level at C_{pin}=10 pF seems to be larger by five times than that evaluated in [8]. However, by comparison, that value is only at a specific point of bandwidth (10 MHz) and the level of noise increase rapidly after and before it to be equal or exceed our simulated noise value.

G. Output Noise Level.

This level defines the RMS sum of all the device contributions propagated to a specified output net [12]. Output net in our buffer is that attached to load resistance or capacitance. Many sources of noise through the devices were simulated. For example, diodes have separate noise contributions from thermal, shot, and flicker noise [12]. This is done for all parts of our circuit. Simulation conditions and values are set as mentioned in Sec. III-A with C_{pin} = 10 pF.

The buffer shows a very small output voltage noise level, Fig. 17 in a wide operating bandwidth and at 100 MHz is 127.94 $pV/(Hz)^{0.5}$. This value is very small indicating that due to simplicity of the present buffer, a very small noise will be transferred in the following attaching circuits. However, the price is paid for such low noise level in the small gain current introduced by the buffer and can expect that, to improve the gain additional

circuits must me added and consequently more noise. So, a compromise between these two situations must be done before designing an effective outdoor WOC receiver.

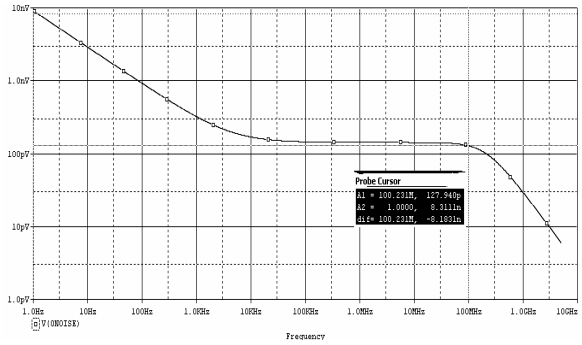

Fig. 17 Output noise level for CCII buffer.

IV. CONCLUSION

This work is very important to answer a part of the WOC outdoor applications. We believe that the use of the described buffer attached to a high gain transimpedence amplifier can enhance the receiving characteristics of any outdoor WOC receiver making it possible to get advantage of a part of the huge optical domain properties. This work can help designers of outdoor practical optical receivers to handle signals with a huge knowledge about variable affecting parameters and how to deal with.

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