A novel power converter with voltage boosting capacitors for a four phase SRM drive

Authors : Y.G. Dessouky* and B.W. Williams**

Dept. of Computing & Electrical Engineering

Heriot-Watt University

Riccarton, Edinburgh

EH14 4AS, U.K.

*** e-mail : ygd@cee.hw.ac.uk**

**** e-mail : bww@cee.hw.ac.uk**

Fax : (+44)-0131-451-3327/3431

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- Abstract

This paper presents a method of enhancing the performance of a four phase switched reluctance motor by using capacitors to produce additional supply voltage during the rise and fall periods of a motor phase current. The voltage rating of the inverter components increases and extra capacitor/diode combinations are needed. The operation and analysis of a series voltage boost circuit are detailed for different modes of operation with a study of the effect of the boost capacitor voltage on the current waveform. Different voltage boost circuit configurations are compared. The predicted and measured results show that the boost circuit increases both torque and output power and, improves the efficiency of the machine, especially at high speeds.

Keywords: power converter, voltage boosting, SRM, drives

List of symbols

C : boost capacitor, F

D : inductance rate of change, $H.s^{-1}$

i : instantaneous phase current, A

I_m : flat-top level of the phase current, A

L : phase inductance, H

L_u : phase inductance at the unaligned position, H

L_a : phase inductance at the aligned position, H

N_r : number of rotor poles

R : resistance per phase, Ω

V : dc supply voltage, V

v_c : instantaneous voltage across the boosting capacitor, V

V_{co} : initial voltage across the capacitor, V

θ : rotor position with reference to the unaligned position, rad

θ_r : rise angle of the current, rad

θ_f : fall angle of the current, rad

θ_d : discharging angle of the capacitor, rad

ψ : phase flux linkage, V.s

ω : rotor angular velocity, rad.s^{-1}

1. Introduction

Switched reluctance motor (SRM) drives have been researched in the areas of motor principles, operation and control [1,2,3]. Because of their cost advantages and ruggedness, these drives are suitable for high speed applications. In this paper a new power converter is presented that improves the high speed performance of a 4-phase SRM, by connecting capacitor/diode parallel combinations in series with the dc link. The capacitor stores the energy recovered from the phase winding during the current fall and pumps the stored energy back into the motor during current rise. This stored energy provides a boost voltage which squares-up the current waveform, hence increases the output power of the motor. This is particularly true at high speeds. Use of the voltage boost circuit has enhanced the performance of single phase [4,5] and two phase [6] SRMs. Separate boost circuits have been employed in three or more phases [7]. For SRMs with three or more phases, it is not possible to use a single boost circuit since over lapping phase currents prevent boost voltage build-up. In this paper the boost circuit in figure 1 uses two capacitors and two diodes with a 4-phase SRM. Details of the SR motor are given in table 1. The six-switch power converter [8] consists of two bridges where quadrature phases share a single-ended bridge leg. With such

an arrangement only one phase current flows through any switch at any time. The converter is suitable for boost circuit adaption because the currents in phases 1 and 3 are 180° electrically separated as are the currents in phases 2 and 4. Therefore, each boost capacitor experiences a periodic current comprised of the two separate, individual currents. A model of the motor with and without the boost circuit, as derived from its differential equations, is presented. The three operating modes of the boost circuit are explained with a study considering the effect of the boost capacitor voltage on the current waveform. Experimental results are presented and performance curves are given. Boost circuits using two capacitor/diode combinations in parallel and using only one capacitor/diode combination in series are also considered.

2. Simulation of the SR drive

2.1 Inductance modelling

In an SRM, the inductance per phase changes from a minimum value, L_u, at the unaligned position to a maximum value, L_a, at alignment. The unaligned inductance is constant (current independent) since the magnetic circuit is dominated by large interpole air gaps. The aligned inductance is a function of current because of saturation effects in the iron parts. Using curve fitting techniques on the flux linkage versus current data, the aligned inductance, L_a, as a function of the instantaneous phase current can be modelled as:

$$L_a(i) = \begin{pmatrix} 216.17 & i < 2.25 \\ 225.08 - 3.96\,i & i \geq 2.25 \end{pmatrix} \quad \text{(mH)} \qquad (1)$$

If the inductance change from the unaligned to the aligned position is approximated by a co-sinusoidal waveform, the instantaneous inductance as a function of the rotor position is given by:

$$L(\theta, i) = \left(\frac{L_a(i) + L_u}{2}\right)(1 - \cos(N_r\theta)) \qquad (2)$$

where the rotor position is related to time by:

$$\theta = \omega t \tag{3}$$

The inductance rate of change is given by:

$$\frac{dL}{dt} = D(t,i) = \left(\frac{L_a(i) + L_u}{2}\right) N_r \, \omega \sin(N_r \omega t) \tag{4}$$

During simulations, the inductance L and its rate of change D (eqn (1) to (4)), are updated for each instantaneous value of current and time.

The instantaneous torque per phase, T_t , is given by:

$$T_t = \frac{1}{2} i^2 \frac{D}{\omega} \tag{5}$$

where the phase produces positive torque when the inductance rate of change is positive. The ideal current during this period, for maximum torque, given a maximum current limit, is rectangular but this is not possible practically. In practice both current rise and fall rates are limited by phase inductance and finite forcing voltages. Therefore, to obtain optimal torque from the motor, the phase current should rise from zero at the unaligned position to reach its flat-top level I_m in the minimal rise angle θ_r. Then it is kept constant at this level until the fall angle θ_f , when the current starts to fall, reaching zero at the aligned position. The rise and fall angles are dependent on machine parameters as well as the operating conditions.

2.2 Current prediction without a voltage boost circuit

The current rises when the phase experiences a positive voltage via switches T_1 and T_{13}, figure 2a. The Kirchhoff's emf equation is:

$$V = i R + \frac{d\Psi}{dt} \tag{6}$$

and flux linkage is related to current by:

$$\Psi = L\,i \tag{7}$$

Substituting (7) into (6), and rearranging gives:

$$\frac{di}{dt} = \frac{V - i\,(R + D(t,i))}{L(t,i)} \tag{8}$$

The current falls when the phase experiences a negative voltage via diodes D_1 and D_{13} (figure 2b) and the emf equation becomes:

$$-V = i\,R + \frac{d\Psi}{dt} \tag{9}$$

Substituting (7) into (9) and rearranging gives:

$$\frac{di}{dt} = \frac{-V - i\,(R + D(t,i))}{L(t,i)} \tag{10}$$

For low speeds, the back emf $d\Psi/dt$ is small and therefore the current can be maintained at the flat-top level I_m by alternatively chopping the current in positive voltages loops (figure 2a) and zero voltages loops (figure 2c). The higher the speed, the higher the back emf and consequently the rise angle θ_r increases and the fall angle θ_f decreases, converging to the crossover speed ω_1 when $\theta_r = \theta_f$. For speeds higher than ω_1, the current does not reach I_m but attains a smaller value I_e. To find the current waveform for different speeds, the rise and fall angles are determined by solving the non-linear differential equations (8) and (10) respectively. The necessary boundary conditions are given in table 2.

2.3 Current prediction with a voltage boost circuit

The current rises when the phase experiences positive voltage loops (figure 3a) while the boost capacitor is discharging. The emf equation is given by:

$$V + v_c = i\,R + \frac{d\Psi}{dt} \tag{11}$$

Substituting (7) into (11) and rearranging yields:

$$\frac{di}{dt} = \frac{V + v_c - i\,(R + Dt,i))}{L(t,i)} \tag{12}$$

The boost capacitor voltage is related to the current by:

$$\frac{dv_c}{dt} = -\frac{i}{C} \tag{13}$$

The current falls in negative voltage loops (figure 3b) thereby charging the boost capacitor. The emf equation is given by:

$$V + v_c = -iR - \frac{d\Psi}{dt} \tag{14}$$

Substituting (7) into (14) and rearranging:

$$\frac{di}{dt} = -\frac{V + v_c + i\,(\mathrm{R} + \mathrm{D(t,i)})}{\mathrm{L(t,i)}} \tag{15}$$

The boost capacitor voltage is related to the current by:

$$\frac{dv_c}{dt} = \frac{i}{C} \tag{16}$$

To obtain the current waveform, equations (12), (13), (15) and (16) are solved. The necessary boundary conditions are speed dependent, as will be shown in section 3. It is assumed that during phase current rise periods switching is dominated by positive voltage loops, whilst during current fall periods the switching duty cycle is dominated by negative voltage loop operation.

Having determined the current waveform either with or without the voltage boost circuit, the torque, input power, output power and the efficiency can be calculated [9,10].

3. Operation modes with the voltage boost circuit

The voltage boost circuit has three modes of operation. Figure 4 shows phase current and the capacitor voltage waveforms for these modes which are explained as follows:

3.1. Operation in mode (1)

As shown in figure 4a, with an initial voltage V_{co} across the boost capacitor at the unaligned position the phase current starts to rise in positive voltage loops (figure 3a). The current reaches I_m at the rise angle θ_r while the capacitor does not discharge completely. The current

is alternately chopped in zero voltage loops (figure 3c) and positive voltage loops (figure 3a). Thus, in every positive voltage loop the capacitor is discharging while in the zero voltage loop the capacitor voltage remains unchanged. This process is repeated until the capacitor voltage reaches zero at the discharged angle θ_d. Then, the boost circuit diode prevents the boost capacitor from charging negatively and it facilitates the positive loop current (figure 3d). The current is chopped to maintain a flat-top level I_m until the fall angle θ_f. The current then falls in negative voltage loops (figure 3b) charging the capacitor. The phase current reaches zero at the aligned position, the capacitor voltage having reached V_{co} which is the initial voltage for the next current cycle. At low speeds, a sufficiently long flat-top current period exists to fully discharge the boost capacitor. This mode continues as the speed increases, until $\theta_d = \theta_r$, such that the current I_m is reached just as the boost capacitor voltage reaches zero.

3.2. Operation in mode (2)

In this second mode (figure 4b) the current starts to rise in the positive voltage loops of figure 3a, discharging the capacitor from V_{co} at the unaligned position to zero at a current level I_d , which is lower than I_m. The current continues to rise until θ_r but the positive loop current is supplied via the diode D_5 from the supply V as implied by equation (8). The current is chopped in alternating zero and positive loops as in figure 3c and 3d respectively until θ_f. The current fall period (i.e. $\theta_f \leq \theta \leq \pi/6$) resembles that of mode (1). Increasing motor speed increases the rise angle and decreases the fall angle until the crossover speed ω_1 when the rise angle θ_r is co-incident with the fall angle θ_f.

3.3. Operation in mode (3)

For speeds higher than ω_1, the back emf is high and therefore the current has insufficient time to reach I_m but rather attains a smaller value I_e, as shown in figure 4c. This third mode, in analysis, resembles mode (2) except that no flat topped chopping period exists.

The initial conditions of the differential equations which determine the current waveform for each mode are given in table 3.

4. Effect of boost capacitor voltage on the current

The current waveform depends on the motor operating conditions. The major factor affecting the waveform is the boost capacitance magnitude. As explained in section 3, the rise angle is co-incident with the fall angle at the crossover speed, ω_1, after which the phase current does not reach I_m. Figure 5a shows the relationship between crossover speed and boost capacitance. It is seen that the lower the capacitance, the higher the crossover speed. The maximum phase current is I_m for speeds lower than ω_1 and I_e for speeds in excess of ω_1. The relationship between maximum phase current and speed, shown in figure 5b, indicates that decreased capacitance increases the maximum phase current for high speeds. Decreased capacitance also decreases the rise angle and increases the fall angle for low speeds as shown in figure 5c. From the previous relationships, it is established that the boost capacitance increases the current waveform area and hence developed torque. The maximum voltage across the capacitor is the initial voltage V_{co} at the unaligned position. Thus the maximum reverse voltage across any switch or bridge diode will be $(V+V_{co})$. Figure 5d shows the relationship between V_{co} and speed. It illustrates that the lower the capacitance, the higher the initial capacitor voltage and consequently the higher the necessary voltage ratings of the inverter components.

5. Practical performance of the drive

Figure 6 shows typical experimental phase current and boost capacitor voltage waveforms. The performance of the machine on-load with and without voltage boosting is recorded and compared with the simulation results. Motor speed dependence of developed torque, output and input power and the efficiency are shown in figure 7. It is clear that voltage

boosting increases the output power and enhances the efficiency of the machine, especially at high speeds where the maximum attainable phase current is increased. At a speed of 2000 rpm, a boost capacitance of 10 μF improves output power and efficiency by 25.2% and 8.2% respectively. Differences between calculated and measured performance in figure 7 can be attributed to errors introduced due to the simple model used and the neglect of windage, friction, eddy currents and hysteresis losses.

6. Parallel boost circuit

Figure 8a shows the 4-phase drive circuit with two parallel boost circuits. It has been concluded [6] that the operation of the parallel boost circuit is similar to the series version for single and two phase SRM's. The phase current and capacitor voltage for one bridge of the 4-phase SRM at high speed are shown in figure 8b. The diode D_5 blocks current in phase 1 when the current is falling via D_1 and D_{13}. Therefore the energy in this phase is stored in the boost capacitor such that the capacitor voltage rises from the supply voltage V at point (a) to $(V+V_{co})$ at point (b). The current in phase 3 now rises via T_3 and T_{13}, discharging the boost capacitor to V, whence the diode D_5 comes into conduction at point (c). Then phase 3 is fed directly from the dc supply between time points (c) and (d). Comparing figure 8b with figure 4c, it is seen that for the same capacitance, the motor performance with the series and parallel boost circuits is similar except that the maximum capacitor voltages for the series and parallel connections are V_{co} and $(V_{co}+V)$ respectively. The peak stored energy, hence size for the parallel and series connected capacitors E_p and E_s respectively, are given by :

$$\begin{pmatrix} E_p = \frac{1}{2} C (V_{co} + V)^2 \\ E_s = \frac{1}{2} C V_{co}^2 \end{pmatrix} \qquad (17)$$

The Peak Stored Energy Ratio, PSER, for the same boost voltage, hence capacitance value, can be expressed as :

$$PSER = \frac{E_p}{E_s} = (1+\frac{V}{V_{co}})^2 \quad (18)$$

The physical Size Ratio, SR, related to C×V (viz., Q), is given by:

$$SR = \frac{Q_p}{Qs} = 1+\frac{V}{V_{co}} \quad (19)$$

The relationships between peak stored energy ratio, size ratio and boost capacitance are shown in figure 9. This figure illustrates that advantageously, the stored energy rating and the physical size of the series boost capacitor are always less than that of the parallel capacitor. One advantage of the parallel boost circuit is that the voltage supply need not be a reversible source. This is only important for 1 and 2 phase motors. In higher phase number motors, other conducting phases act as the returned energy sink.

7. Boost circuit using one boost capacitor

Figures 10a and 10b show a boost circuit for the 4-phase SRM drive using only one capacitor/diode combination and the current waveforms respectively. The experimental results confirm that the voltage boost circuit is ineffective. The reason can be attributed to the fact that energy exchange takes place between two conducting phases rather than one phase and the boost capacitor. As shown in figure 10c, for high speeds where boosting is dominant, when the current in phase 2 is falling, the current in phase 1 is rising. Therefore, the recovered energy from phase 2 is divided between phase 1 and the capacitor/supply.

8. Conclusion

The performance of a 4-phase SRM has been enhanced by means of two series capacitive voltage boost circuits. The circuit was modelled for three different operating modes. The study of boost capacitor effects on phase current indicates that decreasing the capacitance increasingly improves performance. However, higher voltage rated inverter components are required. At a speed of 2000 rpm, a 10μF capacitor increases motor output

power and efficiency by 25.2% and 8.2% respectively. Parallel boosting resembles series boosting in analysis but the latter has the advantage of having a lower stored energy, hence lower capacitor voltage rating, for the same value of capacitance. Using only one boost capacitor is not effective because energy exchange takes place between two adjacent conducting phases rather than solely between the phase and the boost capacitor.

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Table 1	
No. of turns per phase = 710	Flat-top current, I_m = 2.4 A
Supply Voltage = 300 V	Phase resistance, R = 9.6
Unaligned inductance, L_u = 79.6 mH	Unsaturated aligned inductance = 216.2 mH

Table 2		$\omega < \omega_1$	$\omega > \omega_1$
	ωt =	i =	i =
Eqn (8)	0	0	0
	θ_r	I_m	I_e
Eqn (10)	θ_f	I_m	I_e
	$\pi/6$	0	0
	-	-	$I_e < I_m$
	-	-	$\theta r = \theta_f$

Table 3	$\omega < \omega_o$			$\omega_o < \omega < \omega_1$			$\omega > \omega_1$		
	ω t =	i =	v_c =	ω t =	i =	v_c =	ω t =	i =	v_c =
Eqn(12),	0	0	V_{co}	0	0	V_{co}	0	0	V_{co}
(13)	θ_r	I_m	$V_x > 0$	θ_d	I_d	0	θ_d	I_d	0
Eqn (8)	-	-	-	θ_d	I_d	-	θ_d	I_d	-

	-	-	-	θ_r	I_m	-	θ_r	I_e	-
Eqn(15),	θ_f	I_m	0	θ_f	I_m	0	θ_f	I_e	0
(16)	$\pi/6$	0	V_{co}	$\pi/6$	0	V_{co}	$\pi/6$	0	V_{co}
	-	-	-	-	-	-	$\theta_r = \theta_f$	$I_e < I_m$	-

List of captions

Figure 1: The voltage boost circuit for a 4-ph SRM drive using two diode/capacitor combinations in series

Figure 2: Phase winding in (a) positive, (b) negative and (c) zero voltage loops

Figure 3: Voltage boost circuit in (a) positive via capacitor, (b) negative, (c) zero and (d) positive via diode voltage loops

Figure 4: Phase current and capacitor voltage waveforms for different modes of operation

Figure 5: The relationship between (a) crossover speed and boost capacitance, (b) maximum phase current, (c) switching angles and (d) capacitor initial voltage versus speed for different boost capacitance

Figure 6: Experimental phase current and capacitor voltage waveforms:

2ms/div, upper trace 1A/div and lower trace 50V/div

Figure 7: Torque, power and efficiency versus speed for different boost capacitance

Figure 8: (a) Circuit diagram and (b) phase current and capacitor voltage waveforms for the parallel capacitor voltage boost circuit

Figure 9: Peak energy stored ratio and size ratio versus boost capacitance

Figure 10: (a) Circuit diagram, (b) current waveforms and (c) energy exchange illustration for the one diode/capacitor voltage boost circuit

Biography:

Yasser G. Dessouky received B.Sc. and M.Sc. degrees from Alexandria University, Egypt, in 1991 and 1993. Since 1991 he has been with the Department of Electrical and Control Engineering of the Arab Academy for Science and Technology, Alexandria, Egypt. He is currently on a Ph.D. programme at in Heriot-Watt University, Edinburgh, U.K. His research interests include microprocessor applications, power electronics and machine drives.

Barry W. Williams received a Ph.D. degree from the University of Cambridge, U.K., in 1980. He has been a Professor of Electrical Engineering at Heriot Watt University, Edinburgh, U.K., since 1986. His research interests include semiconductor device applications and machine drives.