Combining Cyclic Q Delay and Cell Interleaver for Enhanced Performance DVB-T2 System

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ABSTRACT

DVB-T2 (The second generation Digital Video Broadcasting) is mainly aimed to replace the current standard DVB-T. The main motivation of DVB-T2 is to provide broadcasters with more advanced and efficient alternative to DVB-T standards. The cyclic Q delay and the cell interleaver are both optional modules existing in the DVB-T2 system. The main purpose of the two modules is to increase the overall DVB-T2 system performance. In this paper we propose a new algorithm to combine the two modules. The new algorithm serves as a primary verification step before hardware implementation. The aim of the combined module is to decrease the system complexity, hardware usage and the overall system delay.

KEYWORDS

DVB-T, DVB-T2, Cyclic Q delay, Cell Interleaver, Pseudo random Generator

1 INTRODUCTION

DVB-T (Digital Video Broadcasting-Terrestrial) which is a standard for digital terrestrial television broadcast [1] was first published in 1997 and was first used in Sweden and UK in1998. DVB-T2 (The second generation DVB) standard is mainly aimed to replace the current standard DVB-T [2]. The main motivation of DVB-T2 is to provide broadcasters with more advanced and efficient alternative to DVB-T standards. The DVB-T2 is a redefined system that allows a more efficient usage substituting the extremely large DVB-T cost [3].

There have been a tremendous amount of researches in the DVB-T2 area. The authors in [4], [5] proposed new error correction technique which is a combination of both LDPC (Low density Parity Check) and BCH (Bose-Chaudhuri-Hocquengham) employed in DVB-T2. The combination technique was aimed to replace the traditional convolutional and Reed Solomon coding employed in DVB-T. In [6],[7] the authors mainly focused on researching, simulating and testing the BICM (Block Interleaving and Coding Modulation) block in the DVB-T2 system. In their simulation and testing the authors included all possible interleaving, coding and modulation present in any BICM block carried out on a single PLP (Physical Layer Pipe). In [8] the Constellation rotation technique, which was analysed, is one of the features employed in the DVB-T2 system. The constellation rotation is known to increase system robustness. DVB-T2 standard includes two methods for PAPR (Peak to Average Power Ratio) reduction techniques, which are ACE (Active Constellation Extension) and TR (Tone Reservation). The two techniques adopted for PAPR in DVB-T2 system are investigated in details in [9], [10].

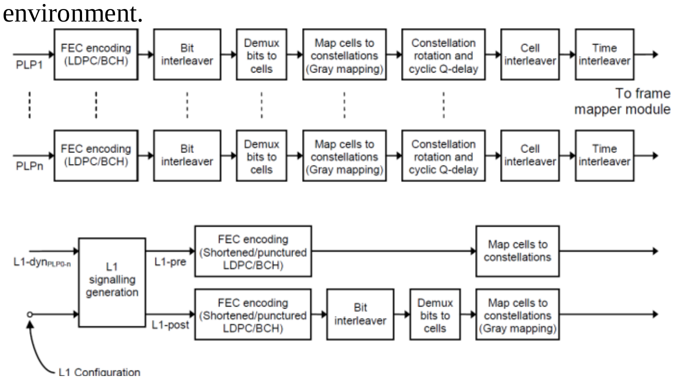
The literature lacks information about efficiently implementing the cyclic Q delay and the cell interleaver modules in a DVB-T2 system.
Thus in this paper we propose a new efficient simulation algorithm that combines both the cyclic Q delay and cell interleaver for the DVB-T2 system. This algorithm serves as a primary step for verification purposes for further hardware implementation.

The paper is organized as follows; we introduce the DVB-T2 system along with a comparison with the previous DVB-T system in section II. Cyclic Q delay and Cell interleaver are presented in details in section III. The proposed technique and Matlab simulation are explained in section IV. Finally a conclusion comes at the end of the paper along with the future work in section VI.

2 THE SECOND GENERATION DVB-T SYSTEM

The DVB Project has developed DVB-T2 standard, its specification was first published in June 2008. The DVB-T2 has been standardised by ETSI (European Telecommunication Standardisations Institute) in September 2009. The main motivation of DVB-T2 is to provide broadcasters with more advanced, efficient alternative to DVB-T standards, substituting the extremely large DVB-T cost. The DVB-T2 common block diagram is shown in fig.1. The DVB-T2 system introduces a new modulation and coding techniques in comparison with DVB-T. In addition, the standard range of COFDM (Coded Orthogonal Frequency Division Multiplexing) parameters has been extended with respect to DVB-T in order to provide a greater flexibility []. The main differences between DVB-T and DVB-T2 are summarized in table.1.

The first module in the system is the input pre-processor, this module converts input data stream into DVB-T2 BB frames (Base Band Frames) [2],[3]. The BB frames are the fed to the FEC coding (Forward Error Correcting). The FEC module consists of two combined techniques which are LDPC [4] and BCH [5]. The combined modules offer a robust signal reception. The output of the FEC module passes through the BICM stage. The BICM stage consists of four interleaving stages for the purpose of achieving a better performance. The first interleaving subsystem module which is the bit interleaver consists of two consequently interleaving process the parity interleaving then the column twist inter- leaving [2]. The output data is then passed through the mapping bits onto constellation module, where gray mapping takes place. The output is then fed to constellation rotation and cyclic Q delay module [8] that was initially suggested in [6]. Worth mentioning that the constellation rotation and cyclic Q delay are optional modules intended to give a better performance in fading environment.



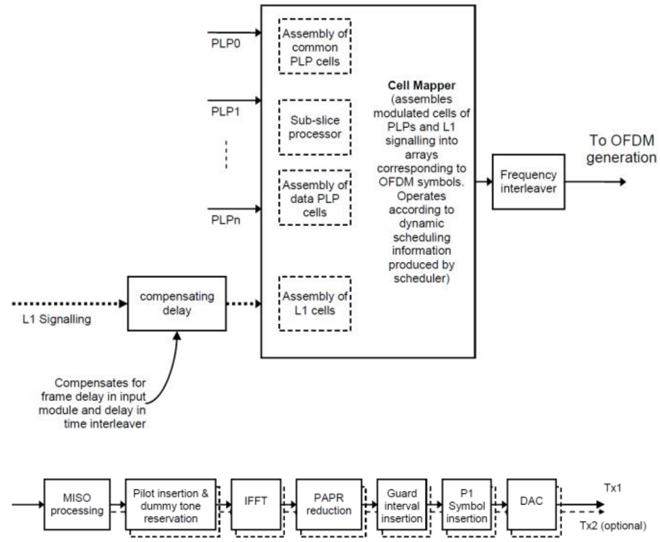


Fig.1 DVB-T2 Transmitter

The output of the data faces another interleaving process. This interleaving process consists of two interleaving stages; the cell interleaving and the time interleaving. The Cell interleaver uses a pseudo random generator to randomly spread the coming FEC data block. While, the Time interleaver module builds TI (Time Interleaver) blocks as explained in [2]. The BICM then forwards the data to a cell mapper, The Cell mapper assembles the modulated cells into arrays corresponding to OFDM symbols.

Table.1 The differences between DVB-T and DVB-T2

	DVB-T	DVB-T2
Input stream	Single stream	Multiple stream
Coding and Modulation	Constant	Variable
Forward Error Correction	Convolutional coding + Reed Solomon 1/2, 2/3, 3/4, 5/6, 7/8	LDPC + BCH 1/2, 3/5, 2/3, 3/4, 4/5, 5/6
Modulation Schemes	QPSK, 16QAM, 64QAM	QPSK, 16QAM, 64QAM, 256QAM
Modulation	OFDM	OFDM
Guard Interval	1/4, 1/8, 1/16, 1/32	1/4, 19/256, 1/8, 19/128, 1/16, 1/32, 1/128
Scattered Pilots	8% of total	1%, 2%, 4%, 8% of total
Continual Pilots	2.6% of total	0.35% of total
DFT	2k, 8k	1k, 2k, 4k, 8k, 16k, 32k

The output is then handed to a frequency interleaving module. The frequency interleaver main role is to operate on the data cells of each OFDM symbol and to map them from the frame builder onto available data carriers [2]. The pilot insertion module is then used whose function is similar to the DVB-T system. The signal is then converted from the frequency domain to the time domain by using the IFFT (Inverse Fast Fourier transform) operation, PAPR reduction techniques are employed on the resulting stream, then guard interval is inserted [2]. Finally, the signal undergoes digital to analogue and carrier modulation, so that the DVB-T2 signal is ready for broadcasting.

3 CYCLIC Q DELAY AND CELL INTERLEAVER MODULES

In this section we discuss in details the role of both cyclic Q delay and cell interleaver modules in a DVB-T2 system.

3.1 Cyclic Q delay

Cyclic Q delay is one of the optional modules that is used in DVB-T2. The main role of the cyclic Q delay module is to uncorrelate the real and imaginary parts (in-phase (I), quadrature (Q)) components of every constellation point especially in severe fading environment [2]. The cyclic Q- Delay works on the constellation rotated data $Cin=(Cin_1, Cin_2, \ldots, Cin_{Ncells})$ and it delays the imaginary part by one cell. N_{cells} is the number of cells per FEC block. The output of the cyclic Q delay is referred to as $Co= (Co1, Co2\ldots, Co_{Ncells})$, where Co is given by:

$$Co = Re(Cin_i) + j\ Im(Cin_{i+1}) \quad (1)$$

Where i takes on the values 1, 2, 3 … N_{cells}. Fig.2 gives an illusteration for the operation taking place in cyclic Q delay.

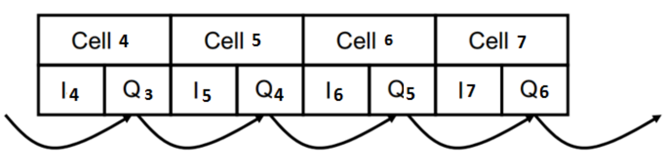


Fig.2 Cyclic Q-delay process

Table.2 cells number relatively to modulation mode

LDPC Block Length	16200				64800			
Modulation Mode	QPSK	16-QAM	64-QAM	256-QAM	QPSK	16-QAM	64-QAM	256-QAM
N_{cells}	8100	4050	2700	2025	32400	16200	10800	8100

3.2 Cell Interleaver

The main goal of the interleaving process is to spread the content in the time/frequency plane, such that neither impulsive noise nor frequency-selective fading would cause a long sequence of the original data stream to be erased [2]. The cell interleaving process applies a pseudo-random permutation in order to uniformly spread the cells in the FEC code word.

The input cells to the cell interleaver take a new index which was generated from the pseudo random process. The Pseudo Random Cell Interleaving process which is done by the cell permutation is used to ensure an uncorrelated distribution of channel distortions in the receiver. The input to the cell interleaver is the data cells $Co= (Co_1, Co_2\ldots, Co_{Ncells})$ which is generated by the constellation rotation and cyclic Q delay process. The output of the cell interleaver is a vector referred to as CIo (j) = $(CIo_{j,1}, CIo_{j,2}, CIo_{j,3},\ldots, CIo_{j,Ncells})$. The vector is defined by: $CIo_{j,Sj(i)=} Co_{j,i}$,where i= 1,2,...,Ncells and Sj(i) is the permutation function applied to FEC block j of the Time interleaver block.

$$S_j(i) = [S_1(i) + P(j)] \bmod N_{cells} \quad (2)$$

where $S_1(i)$ is the basic permutation function and P(j) is the shift value to be used in FEC block j.

The permutation function is based on a maximum length sequence, of degree (Q_n), which is given by the following equation .Worth mentioning that, the address is discarded when it is generated with a value greater than N_{cells}. As in [2] The basic permutation function $S_1(i)$ is defined by the following algorithm:

a) For initializing the pseudo random generator of the basic permutation,

1)the toggling of the most significant bit of binary word Xi is attained by the following equation

$$\text{For } h=1: 2^{Qn}$$
$$X_h(Q_n)=h \bmod 2 \quad (3)$$

2) Initialization of the first two is done by filling $X_h(1:Q_n-1)$ by zeros.

$$\text{For } h=1:2$$
$$X_h(1:Q_n-1)=0,0,0,\ldots,0 \quad (4)$$

3) While the initialization of the third count is produced by filling the most significant bit by one and the rest of the bits by zeros.

$$\text{For } h=3$$
$$X_h(1:Q_n-1)=1,0,0,\ldots,0 \quad (5)$$

b)1) The rest of the counts after the third is obtained by shifting the bits from 2 to Q_n-1 of the present count to take place in location 1 to Q_n-2 bits in the following count. This is defined by the following equation.

$$\text{For } h=4:2^{Qn}$$
$$X_h(1:Q_n-2)= X_{h-1}(2:Q_n-1) \quad (6)$$

Where Q_n-1bit is the result of Xoring different taps depending on the value of Q_n employed as illustrated in table 3.

2) For all X_h if $X_h > N_{cells}$, it is discarded from the output of the pseudo random generator.
3) For every new N_{cells} the pseudo generator adds a new value to the basic permutation $S_j(i)$.It starts by giving a zero value to a variable k also a value of N_{cells} is given to the permutation
$S_j(i)$. While $S_j(i)$ is greater than N_{cells}-1, the permutation will be as shown in the following equation:

$$P(j)=\sum_{t=1}^{Qn}[k-[k/2^{t+1}]/2^{t}]*2^{Qn-t} \quad (7)$$

So for example for using N_{cells}= 10800, 64 QAM, so the shift P(j) to be added to the permutation for j =1, 2, 3, etc. would be 1, 8 193, 4 097, 2 049, 10 241, 6 145, 1 025, 9 217, etc.

Table.3 Xoring tabs

Xoring Tabs	Q_n
1,4	11
1,3	12
1,2,5,7	13
1,2,5,6,10,12	14

Thus the output of the cyclic Q delay is interleaved by the algorithm summarized above as shown in figures (3-6).

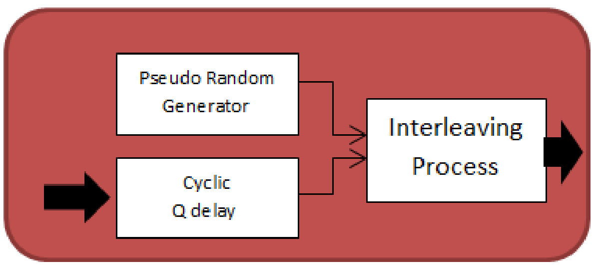


Fig.3 Cell interleaving process

1+2i	3+4i	5+6i	7+8i

Fig.4 Input to the cell interleaver (example)

4	2	1	3

Fig.5 Pseudo random generator output (example)

7+8i	3+4i	1+2i	5+6i

Fig.6 The cell interleaving output (example)

Note that at the receiver side the inverse process for both cyclic Q delay and cell interleaver take place. The inverse process for both modules is illustrated in figures (7-11).

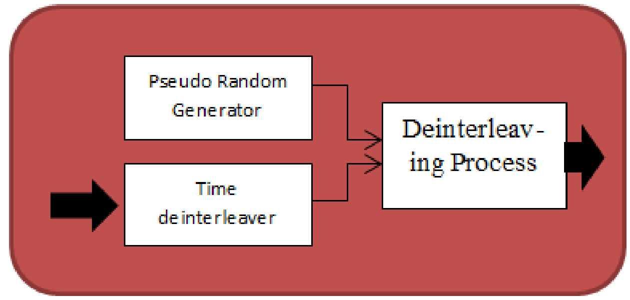


Fig.7 The Cell Deinterleaving process

7+8i	3+4i	1+2i	5+6i

Fig.8 Input to the cell deinterleaver (example)

4	2	1	3

Fig.9 Pseudo random generator output (example)

1+2i	3+4i	5+6i	7+8i

Fig.10 The cell deinterleaving output (example)

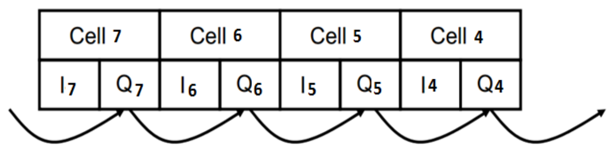


Fig.11 The Inverse cyclic Q delay process

4 Proposed Algorithm and MATLAB Simulation Results

In this section we discuss in details the combined module for both the cyclic Q delay and cell interleaver. The new module serves as a preliminary step for verification purposes prior to hardware implementation. A Matlab program was written for the proposed combined module. The input to the Matlab program is the output cells of the constellation rotation module, while the output of the proposed module is Q delayed cell interleaved cells. A 64 QAM is employed so that 10800 is the number of cyclic Q delay input cells. Note that the program was written for both sides (Transmitter and receiver). The block diagram of the simulation module is shown in fig. 12. Table 4 shows the input to the module while table 6 is the module output in transmitter.

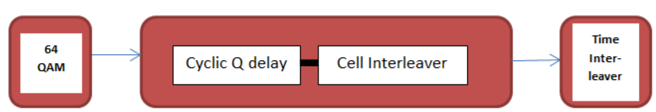


Fig.12 Transmitter proposed algorithm

Table 4 The data input to the proposed transmitter module

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24+ 5.09j	5.98 - 6.17j	-7.96 +5.8j	-3.71 +4.49j	-1.92 +7.36j	3.41- 2.51j	6.77+ 2.03j	-6.1 -5j	1.92+ 7.36j	3.1- 0.5j

L=10800

Cell L-9	Cell L-8	Cell L-7	Cell L-6	Cell L-5	Cell L-4	Cell L-3	Cell L-2	Cell L-1	Cell L
7.96- 5.87j	0.83 - 1.13j	3.71- 4.49j	-3.41 +2.51j	4.01- 6.47j	2.51- 3.41j	0.54+ 3.11	-6.4 -4j	-1.73 +4.79j	-1.4 +2j

Table 5 The Pseudo random generator permutation

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cel l 8	Cell 9	Cel l 10
1	8193	4097	10241	5121	10753	1281	8833	4417	10401

Cell L-9	Cell L-8	Cell L-7	Cell L-6	Cell L-5	Cell L-4	Cell L-3	Cell L-2	Cell L-1	Cell L
963	8674	241	8313	61	8223	16	8200	4	8194

Table 6 The proposed module output

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cel l 8	Cell 9	Cel l 10
0.24+ 2.81j	-4.49 +3.1j	2.51+ 2.03j	2.51+ 3.11j	5.09+ 3.11j	2.21+ 5.39j	1.92- 2.21j	-2.5 -1j	-6.17 + 5.39j	4.7+ 1.1j

Cell L-9	Cell L-8	Cell L-7	Cell L-6	Cell L-5	Cell L-4	Cell L-3	Cell L-2	Cell L-1	Cel l L
7.36+ 7.07j	3.7+ 4.7j	1.92+ 4.16j	-0.24 -3.41j	-6.47 -4.16j	-3.41 -5.09j	2.21+ 7.07j	-4+ 0.05 j	-3.71 +5.87j	3.7- 3.7j

Fig. 13 shows the block diagram of the receiver module along with its input and output respectively in tables (7,8)

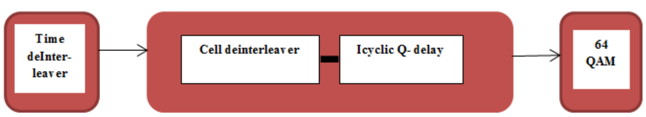


Fig.13 Receiver proposed module

Table 7 The receiver module input

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24+ 2.81j	-4.49 +3.1j	2.51+ 2.03j	2.51+ 3.11j	5.09+ 3.11j	2.21+ 5.39j	1.92- 2.21j	-2.5 -1j	-6.17 + 5.39j	4.7+ 1.1j

Cell L-9	Cell L-8	Cell L-7	Cell L-6	Cell L-5	Cell L-4	Cell L-3	Cell L-2	Cell L-1	Cell L
7.36+ 7.07j	3.7+ 4.7j	1.92+ 4.16j	-0.24 -3.41j	-6.47 -4.16j	-3.41 -5.09j	2.21+ 7.07j	-4 + 0.05j	-3.71 +5.87j	3.7- 3.7j

Table 8 The proposed module output

Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10
0.24+ 5.09j	5.98- 6.17j	-7.96 +5.8j	-3.71 +4.49j	-1.92 +7.36j	3.41- 2.51j	6.77+ 2.03j	-6.1 -5j	1.92+ 7.36j	3.1- 0.5j

Cell L-9	Cell L-8	Cell L-7	Cell L-6	Cell L-5	Cell L-4	Cell L-3	Cell L-2	Cell L-1	Cell L
7.96- 5.87j	0.8+ 1.13j	3.71- 4.49j	-3.41 +2.51j	4.01- 6.47j	2.51+ 3.41j	0.54+ 3.11j	-6.4 -4j	-1.73 +4.79j	-1.4 +2j

CONCLUSION

In this paper we proposed a new simulation that combines cyclic Q delay and cell interleaver in the transmitter and its inverse process of cell deinterleaver and cyclic Q delay removal for DVB-T2 system in the receiver. The proposed module serves as a preliminary step for verification purpose prior to hardware implementation. A matlab code was written to the new combined modules. The simulation results shows that the output of the combined modules are similar to that of the output of the DVB-T2 system cell interleaver. Also,upon reception the received deinterleaved output is similar to that transmitted. Thus, we can conclude that the proposed module is efficiently working and can be further implemented on a FPGA.

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