Implementation of Field Programmable Gate Array (FPGA) for decision making in portable automatic testing systems for IC's library & digital circuits

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***Abstract*:** This paper proposes a real approve design of inexpensive digital circuit testing environment that simplifies functional testing of Integrated Circuits (IC's) and digital circuits. Using this technique will lead to get the decision making if the module is function properly or not. This environment consists of the tester hardware and its corresponding software which enables both engineers and technicians to experience the challenges of testing and debugging without the expense of costly commercial hardware testers. A simple digital circuits is constructed using breadboards, wires, along with Device under Tests (DUT's), then testing using switches and Light Emitting Diodes (LED's). However, advanced digital circuits are often too complex to be tested, and debugged in this way, due to the large amount of states they may require and the larger number of input and output signals compared with simple projects. Moreover the proposed system can be used to test complex digital circuits using image analysis and pattern recognition responses from the DUT compared to the expected stored pattern. Adding to that the system is described as design and implementation of compact, small, cheap for low-power IC_TESTER and digital circuit tester. By implementation of this technique a digital IC tester sends a sequence of test vectors to a DUT, receives the actual response vectors from the DUT, and compares the responses from the DUT to the expected stored response vectors to determine and decide whether DUT is functioning properly or not. So finally we are able to get decision making.

Index Terms- FPGA- IC- Signal Processing- Automatic testing -Digital Circuits- Decision making

I. Introduction

Testing digital circuits for correct operation after manufacturing is an important problem. The problem is how to apply the required test patterns to the Circuit under Test (CUT) and to analyze the response to locate the faulty components so that the circuit board returned to service. The Automatic Test Equipment (ATE) achieves this objective. It produces input test patterns and check binary outputs for correctness. A number of ATE systems are available, the variations are extensive, but most of them fall into two main categories [1]: Functional tester, and In-circuit tester. An in-circuit tester examines each component on the board individually. The in-circuit tester requires a special kind of test fixture to provide electrical connections to all component pins [2]. A functional tester is important to the final user of the circuit board. It verifies that the board performs the functions it was designed for. Only board inputs and outputs need to be tested. The required test fixture is the edge connector that it is inexpensive and simple to construct. The system consists of DUT (4 gates, 2 gates, 3 gates, 6 gates, 5 gates, 1 gate), PC-based logic system which used to download a VHDL written program into a Field Programmable Gate Array (FPGA), and a parallel cable for interfacing which makes the system suitable for either small-scale chip or printed circuit board testing in a quick and efficient usage. The VHDL resulting program can be easily modified and re-downloaded as needed. In this paper, the FPGA implementation uses the Xilinx Spartan-3 chip (XC3S200-FT256) in spartan-3 board of the presented testing architecture. The concept of the portable ATE is presented to reduce the complexity of the traditional ATE [3]. Section 2 presents the concept of ATE architecture. FPGA design steps of the potable ATE will be presented in section 3. The experimental results and the conclusions will be discussed in section 4 and section 5, respectively.

II. Concept of the ATE architecture and hardware implementation of IC TESTER:

The paper proposes the design and implementation of a compact, small, cheap, and low-power IC tester and a digital circuit tester. The system is described as the implementation of a PC-based logic system which used Very High Speed Integrated Circuits Hardware Description Language (VHDL) code program. The system is suitable for either small-scale chip or printed circuit board testing in a quick and efficient usage. The system consists of personal computer (PC), DUT (4 gates, 2 gates, 3 gates, 6 gates, 5 gates, 1 gate), and parallel cable for interfacing. It provides 63 bidirectional input/output (I/O) ports of the FPGA to the DUT which has library of 57 Dual In Package (DIP) chips (14 pin types). It consists of Joint Test Action Group (JTAG) programmer, which has FPGA for downloading the program connected to the electrical erasable programmable Read Only Memory (EEPROM) for storing the bit stream pattern of the correct output of the

devices in the library of the program. It is a small size allowing it to be portable. FPGA- XC3S200-FT256 is used in the system which provides 173 pins in its construction and 120 bidirectional I/O pin to the DUT. EEPROM 2816A (2k) is used which provides 8 bit data path, crystal oscillator 4 MHV for global clock of the FPGA, and 5V power supply for the circuit. The DUT is setup by simply connecting power and ground wires and plugging it into the circuit. Figure (1) shows block diagram of the IC _Tester.

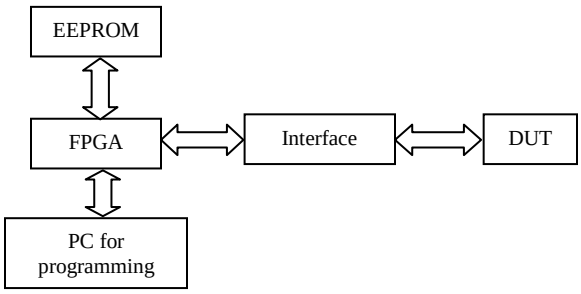

Fig.1. Block Diagram of IC Tester

The construction of the IC TESTER is such that there is DUT and EEPROM, which has the correct output of the ICs in the library, and the FPGA which has a program as a VHDL code, which executes the function of all ICs in the library. The Output Enable (OE) of the EEPROM is connected with 5V and when it is switched to ground, the FPGA read the data from the EEPROM. The clock circuit is connected to the GCK1 (I/O) of the FPGA where 4 MHV crystal oscillator is used as shown in fig.2

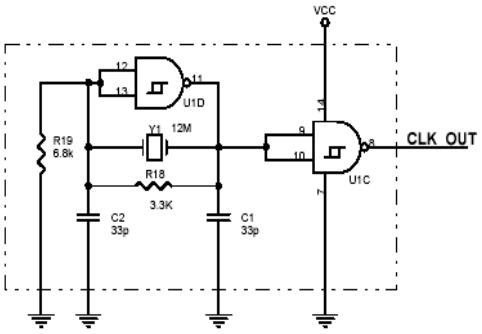

Fig.2. Clock Generator Module for FPGA

After the program downloaded into the FPGA, the DUT is connected to the power supply of the circuit, and the type of the IC (4 gates, 2 gates, 3 gates, 6 gates, 5 gates, 1 gate) can be selected from control lines of the I/O ports of the FPGA. The I/O ports of the FPGA are connected to the address bus and data bus of the EEPROM and are connected to the DUT using buffered interface circuit. When the reset switch connected to the FPGA is pressed, the program will send the Exhaustive ATPG to the input of the DUT and read the output of the DUT to the FPGA, which is compared with correct output of the EEPROM, and get the result of test as a lighting led when the DUT is valid.

III. FPGA design steps of the potable ATE of IC TESTER

Fig.3. Hardware of Spartan-3 Board

The FPGA-based development board provides an inexpensive and expandable platform on which to design and implement digital circuits of all kinds. This board, illustrated in Fig.3 includes hardware of JTAG Parallel Port Programmer.

The Xilinx chip (FPGA XC3S200-FT256), 173 user I/Os, with 200k usable gates, a 4 MHV oscillator

Fig.4 illustrates the block diagram of this portable ATE of the IC TESTER on the Xilinx chip (FPGA XC3S200-FT256).

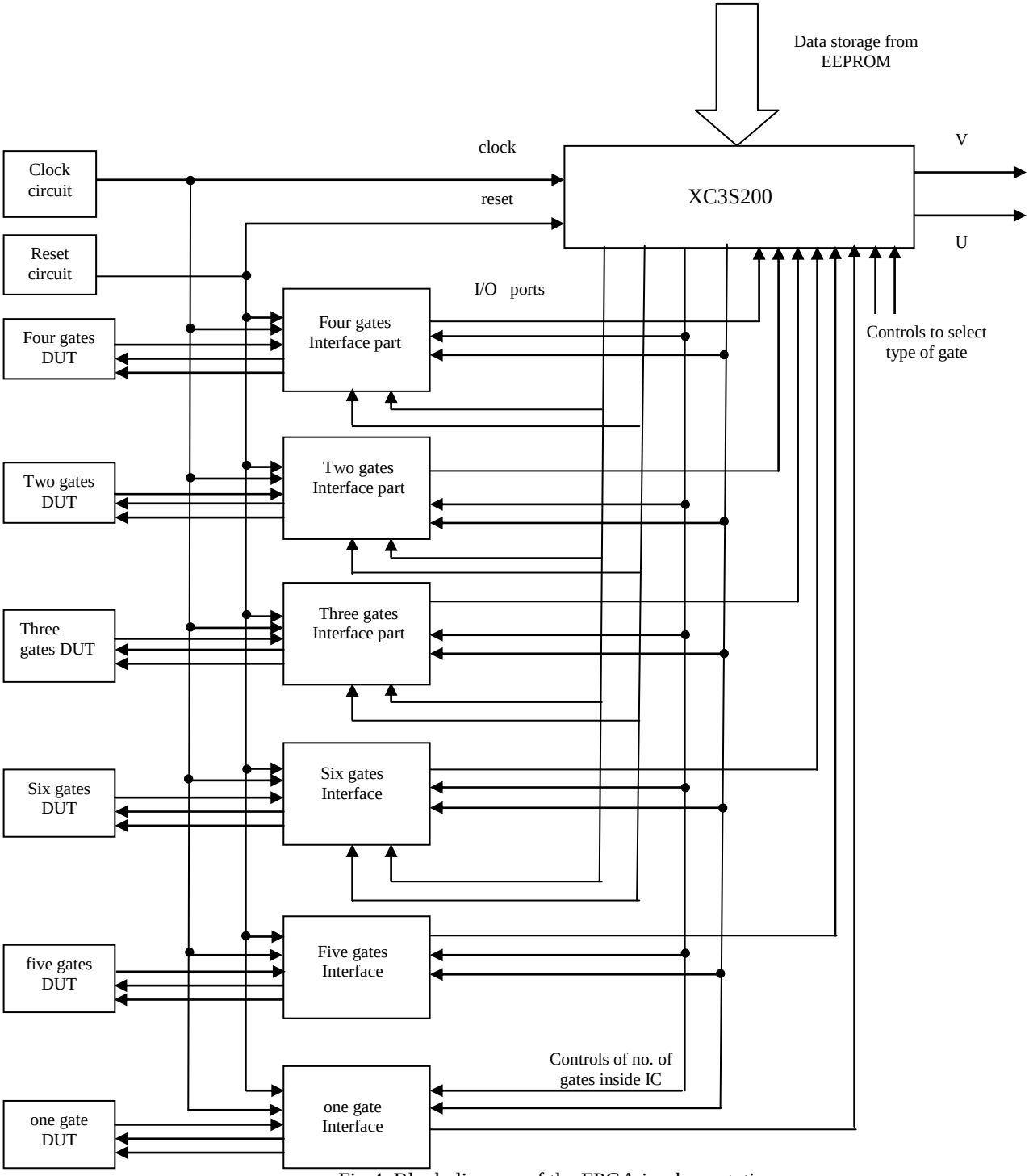

Fig.4. Block diagram of the FPGA implementation
Of the hardware part of the portable ATE of the IC TESTER

III.1 Explanation of the design of the Interface part of 4 gates

This system consists of demultiplexer which selects output control lines connected to tri-state buffers to select the gate which will be tested inside the DUT, and then switched to the next gate according to these output control lines. The multiplexer is used to collect the outputs from the gates and select each of them to the FPGA to be compared to the Correct O/P of the memory is shown in fig. (5)

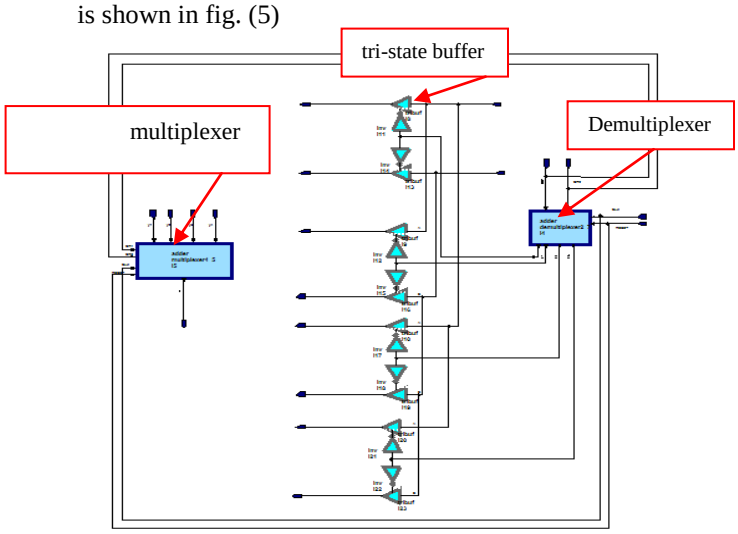

Fig.5. Interface-part of 4 Gates

III.2 Description of state machine of the program

The state machine diagram is used to execute this program. This program checks 4 types of ICs which has 2 gates, 3 gates, 4 gates, 6 gates in its construction

III.2.1 Description of the state machine of 4 gates IC

-When reset=1 and clock is at rising edge, the transition will be at S0 which has 3 control lines (SR1, SR2, SR3) to select between 6 different types of ICs (4 gates, 2 gates, 3 gates, 6 gates, 5 gates, 1 gate)

-When SR1=0, SR2=0 and SR3=0 the transition will be at S1 which has Cr1=0 and Cr2=0 to select between 4 different gates inside IC and which has the first state of the truth table of the input of the first gate of the 4 gates IC.

-When the first bit of the data from the EEPROM k0 = the first output of (y1) from the first gate of the IC, the transition will be at S2 and so on till reach S5 which indicates that the first gate of the IC is finished.

-The control lines will be Cr1=1, Cr2=0 at state S6 because we will start testing the second gate of the IC.

-When the forth bit of the data from the memory k4 = the first output of (y2) from the second gate of the IC, the transition will be at S7 and so on till reach S10 which indicates that the second gate of the IC is finished, and so on till each to S20 which give us the result of testing this IC is valid as a light led when V= 1, Unless the IC will be faulty when U=1 as shown in fig.6

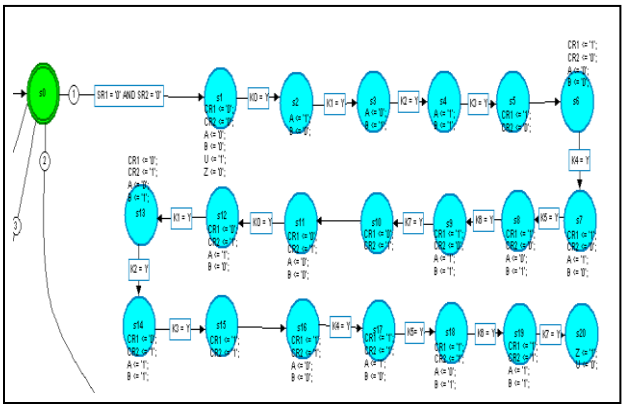

Fig.6. State Machine of 4 Gates IC

The simulation result for 4 gates IC such that 7400 as an example will be indicated in modelsim as shown in fig.7.

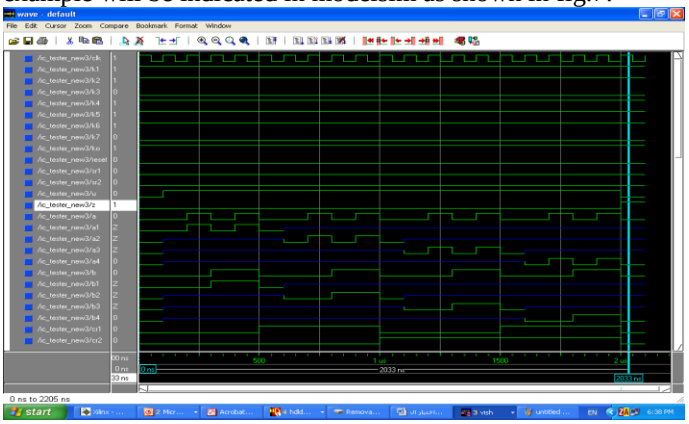

Fig.7. Modelsim Simulation Result

III.3 list of library of the tested ICs

Table.1Library of the Tested ICs

NO	4 gates	5 gates	6 gates	3 gates	2 gates	1 gate
1	7400	7452	7404	7410	7413	7430
2	7402	7453	7405	7411	7420	74133
3	7401	7454	7406	7412	7421	74134
4	7403	7462	7407	7415	7422	
5	7408	7464	7414	7427	7423	
6	7409	7465	7416	7455	7425	
7	7426		7417	7461	7440	
8	7428		7450		7460	
9	7432		7451		74140	
10	7433		7405		74260	
11	7437					
12	7438					
13	7439					
14	7486					
15	74125					
15	74126					
17	74128					
18	74132					
19	74136					
20	74266					
21	74386					

IV. Digital circuit tester

Fig.8 represents a simple Digital circuit which will be tested using exhaustive ATPG which is implemented using VHDL code which is downloaded to XC3S200-FT256.

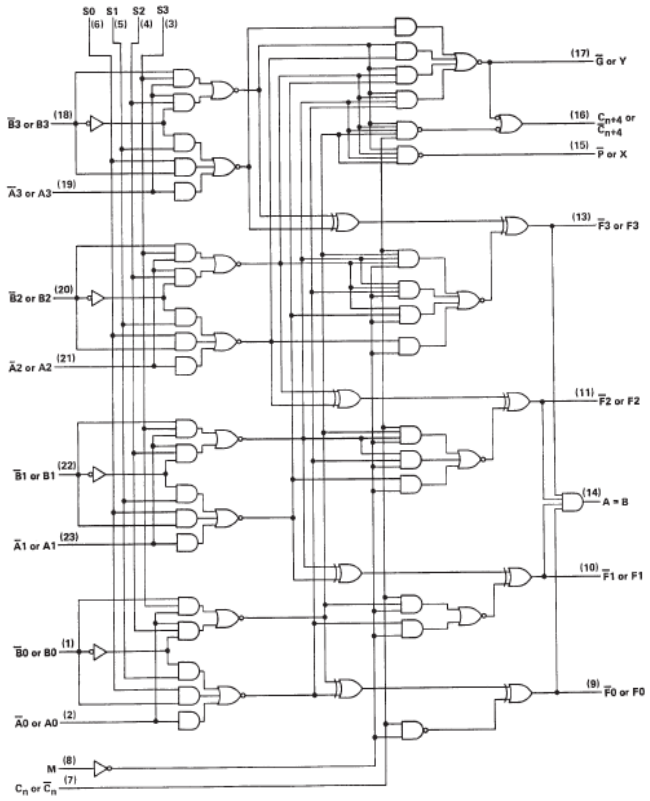

Fig.8. Schematic of Digital Circuit

The function table of the circuit is shown in table.2

Table.2
The Function Table of the Circuit

Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
				Logic	Arithmetic (Note 2)	Logic	Arithmetic (Note 2)
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A}+B$	A + B
L	L	H	L	$\overline{A}+\overline{B}$	$\overline{A}B$ minus 1	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A}+\overline{B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L	H	H	H	$A+\overline{B}$	A + $\overline{B}$	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A}+B$	A plus AB
H	L	L	H	A ⊕ B	A plus B	$\overline{A} \oplus \overline{B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A (Note 1)	Logic 1	A plus A (Note 1)
H	H	L	H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

74181 (4-bit arithmetic logic unit) used in our circuit. it is considered as a block, which its input is clock and reset, and at the output signal V which indicates that the circuit is valid or U which indicates that the circuit is faulty as shown in fig.9

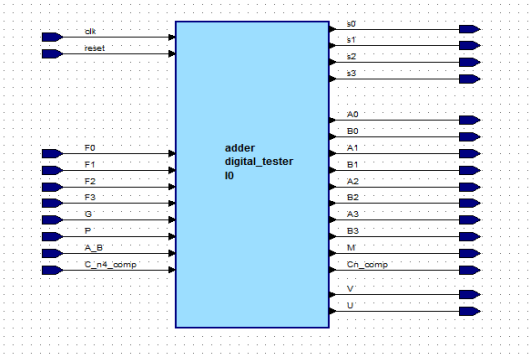

Fig.9. Test Bench of the Circuit using ATPG

IV-2-1 Exhaustive State Machine Description of the Program:

When reset=0 and clock is at rising edge, the transition will be at S0 which has the first state of the truth table of the circuit.
WhenF0=1,F1=1,F2=1,F3=1,G=0,P=0,C_n4_comp=1 and A_B=1the transition will be to S1.
When F0 =0,F1=0,F2=0,F3=0,G=1,P=0, and A_B=0, the transition will be to S2. , and so on till reach S128 which give us the result of checking of this circuit is valid as V =1. Unless it will be faulty when U =1. as shown in fig.10.

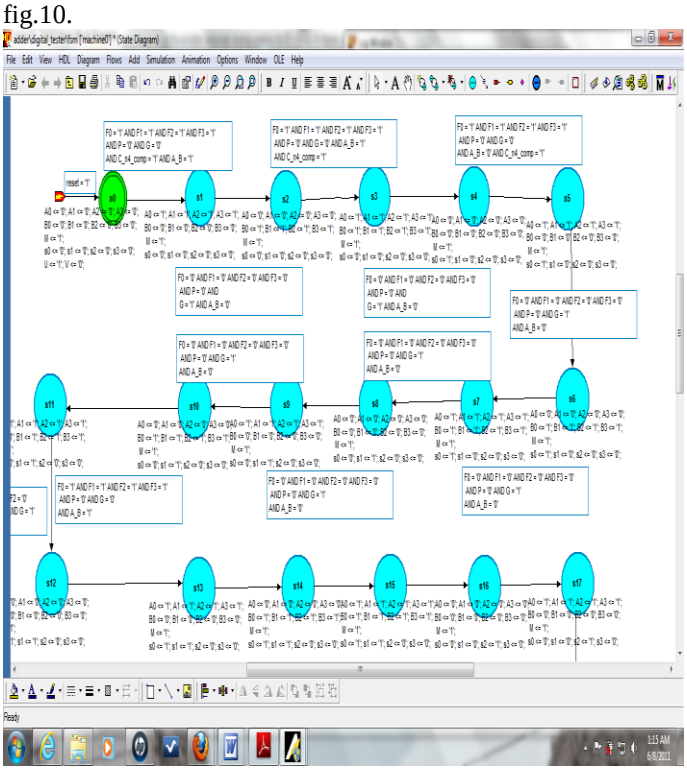

Fig.10. State Machine of the Circuit

IV.2.2 Simulation Result

The clock is at rising edge and reset=0, the program will proceed till reach at the last state which has V=1 to indicate that the circuit is valid .The simulation result will be indicated in modelsim as shown in fig.11.

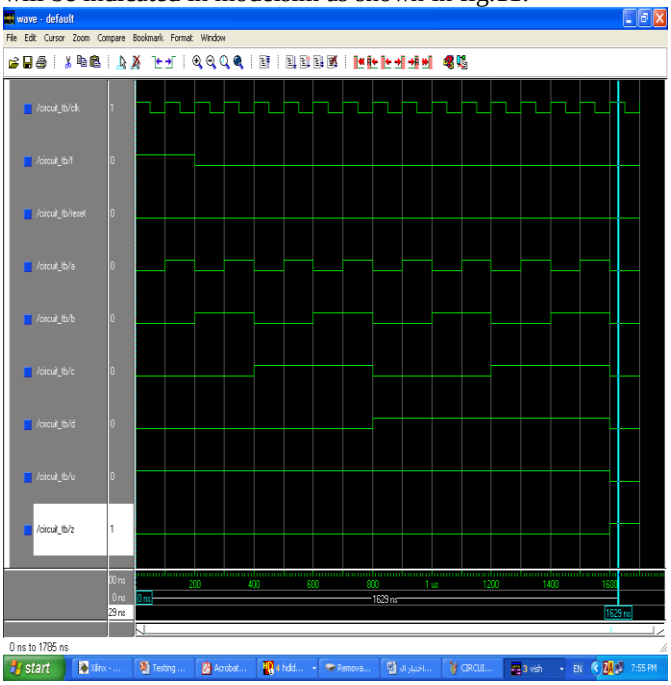

Fig.11. Modelsim Simulation Result

V. Conclusions

The system is inexpensive and versatile for testing chips and both digital circuit boards, and subsystems. The proposed system is used as a hardware test bench using FPGA development environment. Adding to that it can be used as base to test variety of projects using highly integrated logic such as FPLDs, FPGAs, microcontrollers and custom chips.

The implementation of the tester using xilinx FPGA increases the circuit density and reduces the cost, also it can be used to add features and fix design bugs after fabrication of printed-circuit board, moreover FPGA reprogram ability yields to a much more engineer friendly tester. FPGA consume little power in order of only a few milliamperes per pin; the chip xilinx pin driver is protected such that it often prevents the user from destroying a tested chip that was installed or programmed improperly.

The number of wires installed on the tester's socket is limited to the power and ground connections as the tester maps the remainder of the pins through the FPGA. This connection feature improves the setup and reduces the testing time.

The straightforward programming design interface allows the multi use of the design in different cases. Xilinx ISE is the standard user environment for the tester. Parallel cable interface to the host makes the system cheaper.

Applying this system high speed for testing is achieved and can be used to test more complex designs according the requirements using image analysis and pattern recognition of the responses from the DUT compared to the expected stored pattern. Moreover we can conclude that this system and technique can be used in wide scale for any digital circuit's boards.

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